# Class-D Amplifier Project Plan MAY 14-02

#### **Team Members:**

Spencer Bell

**Kyle Shearer** 

Josh Schau

Seth Weiss

Mackenzie Tope

#### Advisor:

Ayman Fayed

# Table of Contents

1.	Executive Summary
2.	Objective Statement
3.	Concept Sketch
4.	Project Schedule4
5.	Work Break Down
6.	Deliverables
	Fall 2013
	Spring 2014
	Specifications
7.	Resource Requirements
	Software5
	Lab Equipment
	Hardware6
	Educational6
8.	Risks
9.	Contact Information7

## 1. Executive Summary

The goal of our team is to design and implement a Class-D Amplifier for audio systems. This type of amplifier has become very popular for typical audio systems because Class- D Amps are very power efficient and can be made relatively small. On top of designing the amp we will also be implementing a 3- Band Equalizer to level out the frequencies coming from the audio source that will improve the sound quality.

# 2. Objective Statement

Our team will be competing in the TI Innovation Challenge. This contest is for senior design students at colleges across the country. The contest requires that we be registered students at an accredited engineering university. We will be judged on the originality, complexity, and quality of our design as well as thoroughness of the written documentation. The judges are also giving points based on the percentage of TI parts used in the design and also require a video demonstrating the working design.

## 3. Concept Sketch



# 4. Project Schedule

Date		Plan of Project Progress	Issues and Set Backs
Sep 9 - 13	Week 1	Research Class D amplifier to form a good understanding of the project.	
Sep 16 - 20	Week 2	Formulate a general schematic and create a spice simulation of the amplifier and equalizer.	
Sep 23 - 27	Week 3	Analyze amplifier schematic and find ways to improve current design. Continue to work with spice model.	
Sep 30 - 4	Week 4	Build a prototype triangle wave generator.	
Oct 7 - 11	Week 5	Generate PWM by using triangle wave generator and a comparator.	
Oct 14 - 18	Week 6	Add power MOSFETs to prototype to be driven by PWM. Design and add an output filter.	Significant shoot-through current when driving the MOSFETs.
Oct 21 - 25	Week 7	Create a Full Bridge version of the current design.	
Oct 28 - 1	Week 8	Design non overlapping clock and test a prototype.	
Nov 4 - 8	Week 9	Design 3 Band equalizer. Add MOSFET drivers to prototype to improve performance.	
Nov 11 - 15	Week 10	Build prototype 3 band equalizer. Change non overlapping clock design.	Previous non overlapping clock design added distortion.
Nov 18 - 22	Week 11	Test new overlapping clock design on amplifier.	
Nov 25 - 29	Week 12	Finalize Schematic of Class D amplifier and 5 band equalizer.	
Dec 1 - 6	Week 13	Start PCB design	
Dec 9 - 13	Week 14	Finish PCB design and Bill Of Materials. Order PCB and components.	

# 5. Work Break Down

Name/Role	Task	
Spencer	Coordinate between subgroups and provide	
Team Leader	theoretical background and research when needed.	
Mackenzie	Main amplifier design research and development.	
Amp designer		
Josh	Assist with amplifier design research and	
Assistant amp designer	development.	
Seth	Research and develop the equalizer system.	
EQ designer		
Kyle	Assist with the researching and development of the	
Assistant EQ designer	equalizer system.	

# 6. Deliverables

#### Fall 2013

By the end of the fall semester we should have implemented a whole system design and have begun prototyping if not finished. We will need to hand in two versions of our design and plan documents and make a slideshow to use during our presentation. We will need to have material to present for 5 minutes in class and then 20 minutes to the reviewers.

#### Spring 2014

At the end of the spring semester our whole design should be finished. This includes a working amplifier and equalizer on a PCB and final versions of our documentation.

#### Specifications

Class D amplifier and 3 Band equalizer. The amplifier must meet the specifications of having a stereo output, 80% power efficiency and a signal to noise ratio of 96dB. The whole circuit should be manufactured onto a single PCB of an appropriate size.

Design document which will include a detailed description of how the amplifier was designed. It will also contain details on specifications, performance, parts used and the thought process behind each sub component of the amp will be included. The design document should also highlight alternative ways the amplifier may have been designed and give reasons as to why they were not chosen. The design document must contain full schematics and parts lists of the amplifier. Sections on testing must show how the amplifier performs under normal conditions as well as under stress.

## 7. Resource Requirements

#### Software

- Multisim
- LT spice
- Matlab
- Free PCB

#### Lab Equipment

- Function generator
- Oscilloscope
- Bench power supply
- Multi-meter

#### Hardware

- Power Supplies
- Power MOSFETs
- Audio op amps
- Comparators
- Gate driver
- Discrete components
- PCB
- Speakers

#### Educational

- Dr. Fayed
- Online power electronics courses
- Tutorials by TI / IR
- Textbooks specifically Sedra/Smith

### 8. Risks

The biggest risk we have to worry about is the parts we buy. Because we cannot physically test the parts we purchase, we have to rely on datasheets and our own ability to pick optimal components. If we purchase components that aren't optimal, we could lose some efficiency and SNR or the system may not function at all.

Poor testing techniques and procedures could cause destruction of the circuit elements we have purchased. We must be careful when we test and buy extra components, so if parts are blown out we do not have to wait and order new parts.

There is some physical risk, in that we will be using power from a wall circuit. In order to operate, our system requires high voltages which introduce the risk of electric shock.

## 9. Contact Information

Spencer Bell ssbell@iastate.edu 319-310-4980

Seth Weiss sgweiss@iastate.edu 515-203-1967

Josh Schau jmschau@iastate.edu 563-260-8902

Mackenzie Tope mktope@iastate.edu 515-520-7714

Kyle Shearer kshearer@iastate.edu 515-520-2586