Simultaneous Co-Test of High Performance DAC—ADC Pairs

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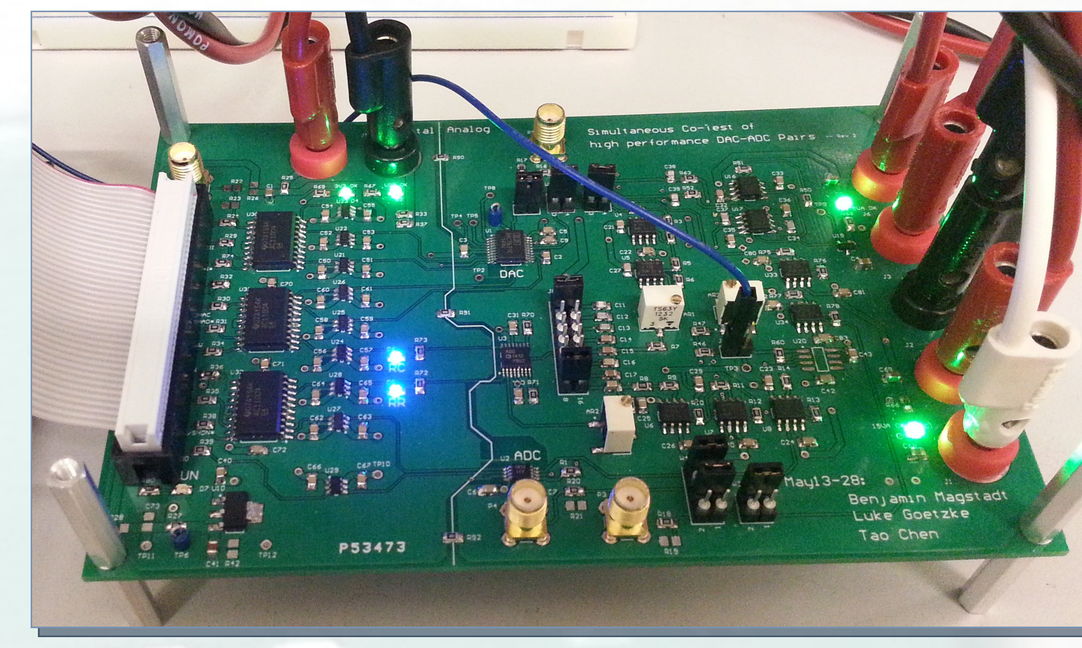


Abstract

In this project a low cost tester was created for simultaneously testing a Digital to Analog (DAC) and Analog to Digital (ADC) converter pair. A significant portion of their part cost comes from the time and money invested in verifying their functionality. Traditional testing methods can take a long time and use costly precision equipment. In the designed system, a DAC is used to generate a sinusoidal wave which passes through two different filters; the ADC digitizes the wave then returns it for processing. The signal in this path acquires non-idealities from the DAC and ADC individually. Ongoing research is indicating that detailed analysis can isolate the DAC's and ADC's non-idealities individually from the overall signal. Having the ability to simultaneously test high performance DAC and ADC pairs will greatly reduce test cost by removing the need for high performance devices, test time by testing the two together, reduce the analysis to purely digital, and eventually overall part cost.

This project was successful and was designed for the purpose of providing a way to collect data for future verification of the analysis algorithm. The tester includes a PCB that houses the converters and necessary filters, and is controlled by a FPGA.

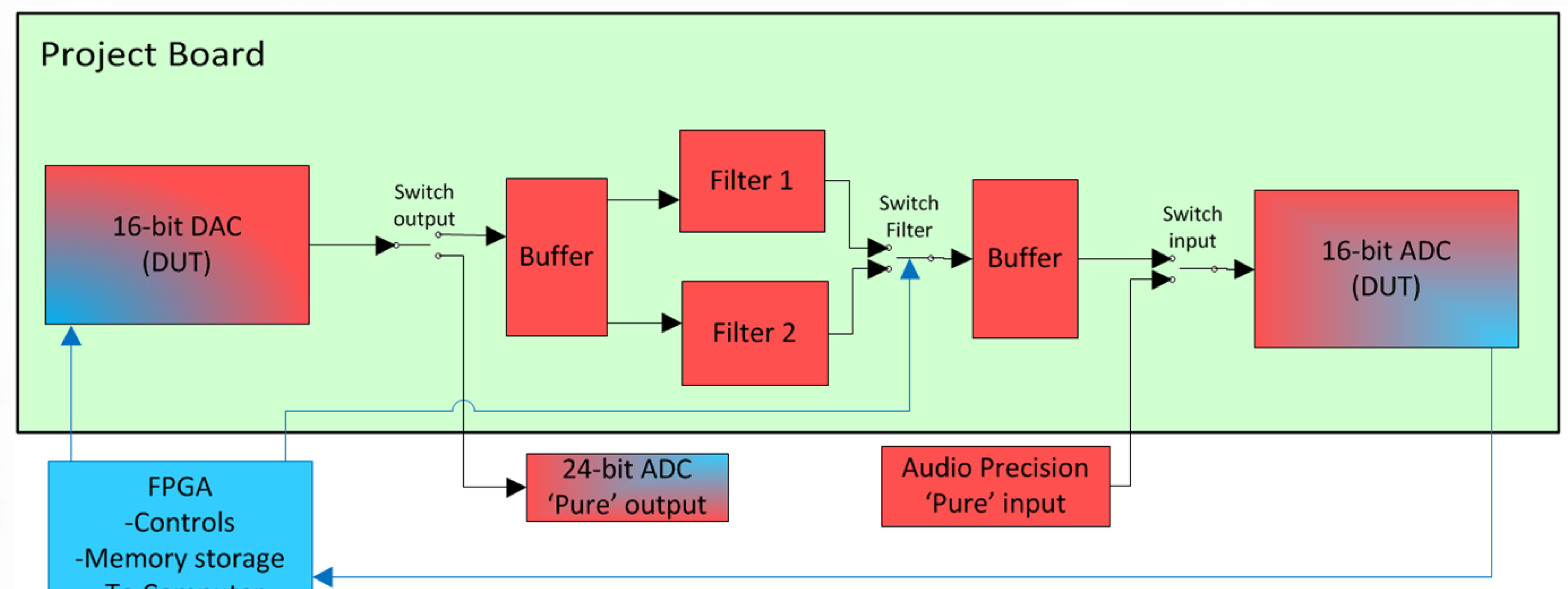


Figure 1: Process flow of the designed PCB, with respect to the FPGA. Complete design is shown in Figure 2. In this diagram red indicates analog signals, while blue indicates digital signals. A block description is provided above.

16b DAC	DAC7631 (100k SPS)
Buffer 1	Isolate DAC from filter
Filter 1	RC filter, phase shift output
Filter 2	Atten. Filter, match amplitude of Filter 1
Buffer 2	Isolate ADC from filter
16b ADC	ADS8321 (100k SPS)
FPGA	40 pin connector cable; digital GPIO
24bit ADC	Method to precisely characterize the DAC
Audio Precision	Method to precisely characterize the ADC

Project requirements as follows:

Functional
- 100k SPS DAC/ADC
- 16 bit precision parts
- Low noise & offset in filter design
- Comparable data to standard test methods

Non—functional
- Low Cost Design
- Modular
- reconfigurable
- easily redesigned
- Small, debugable and reusable

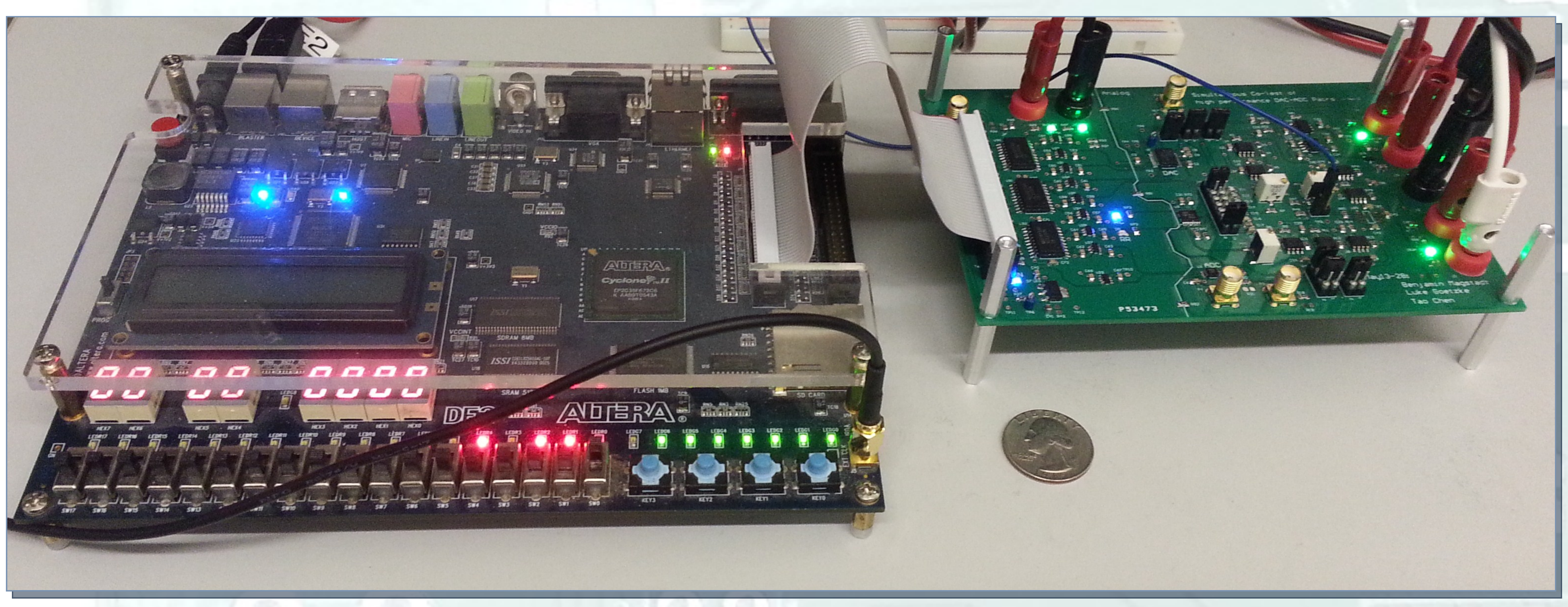


Figure 2: Altera Cyclone II FPGA DE2 board with on board memory chips (left) - programmed in Verilog. Designed DAC-ADC PCB board connected to FPGA (right). The block diagram is described in Figure 1, with the design requirements on the far right.

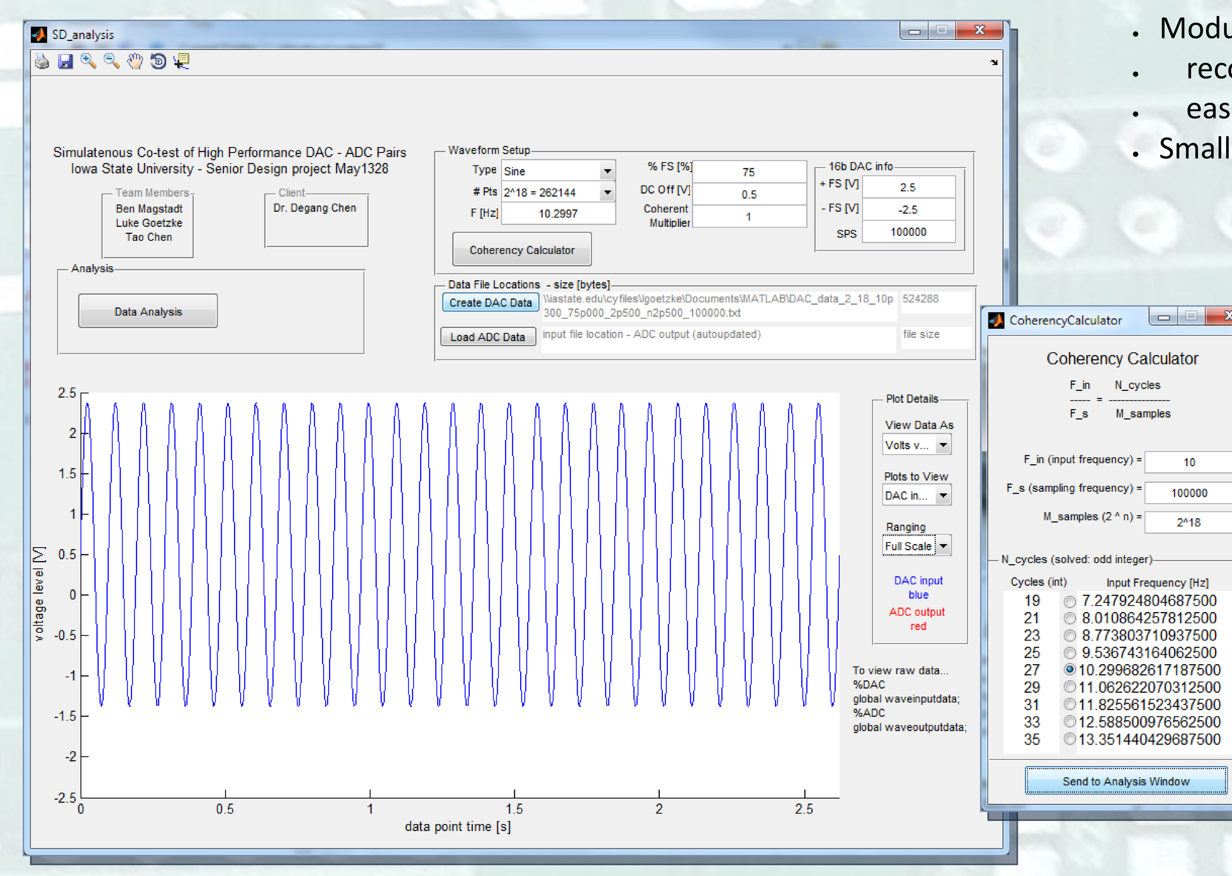
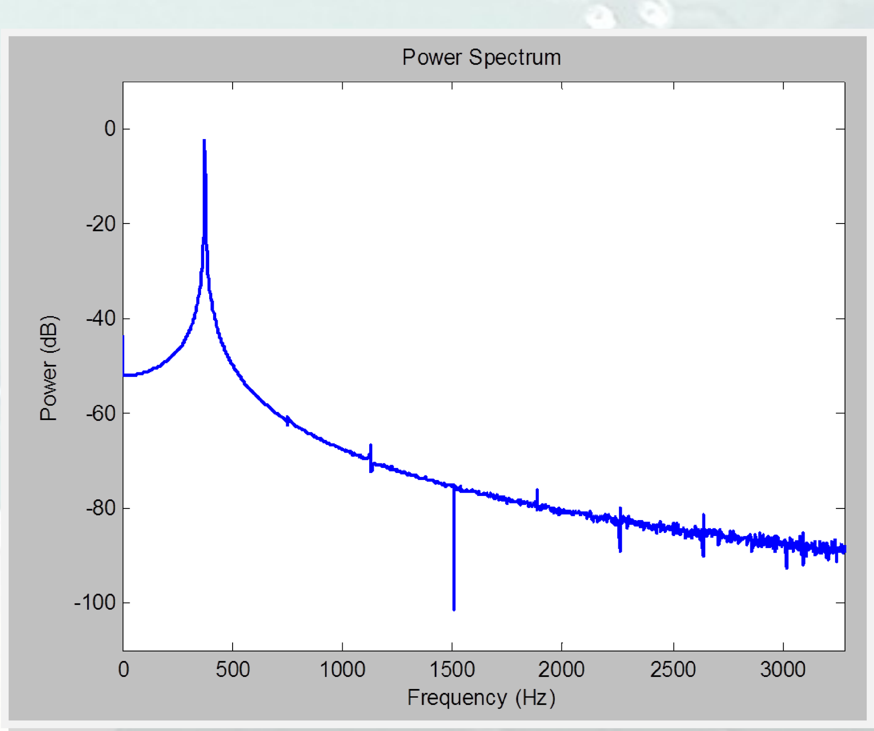
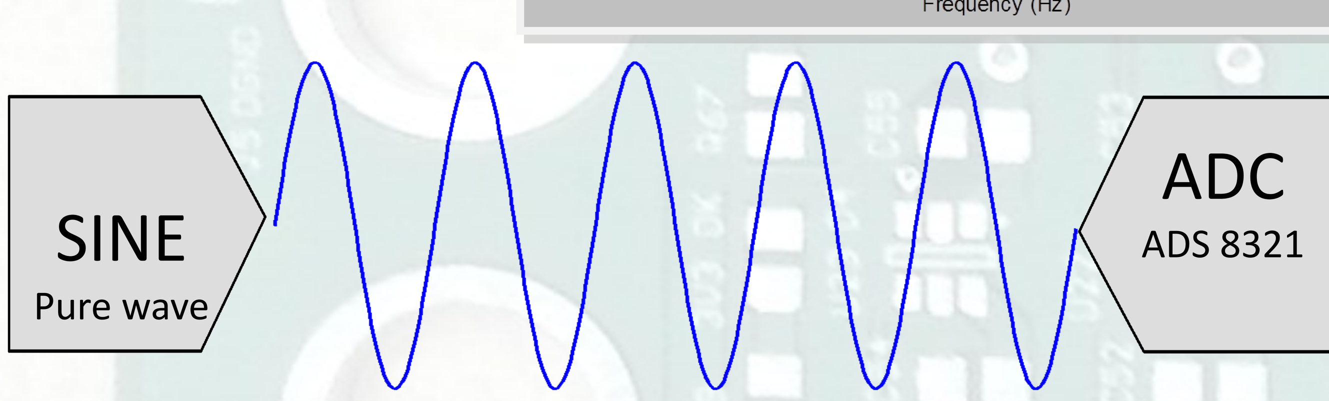


Figure 3: Matlab user interface. This allows the user to create a waveform data file with any number of characteristics. This is sent to the FPGA in Figure 2. The input and output waves are easily viewed here. Shown also is the Coherency Calculator to obtain the required frequency for coherent data sampling.

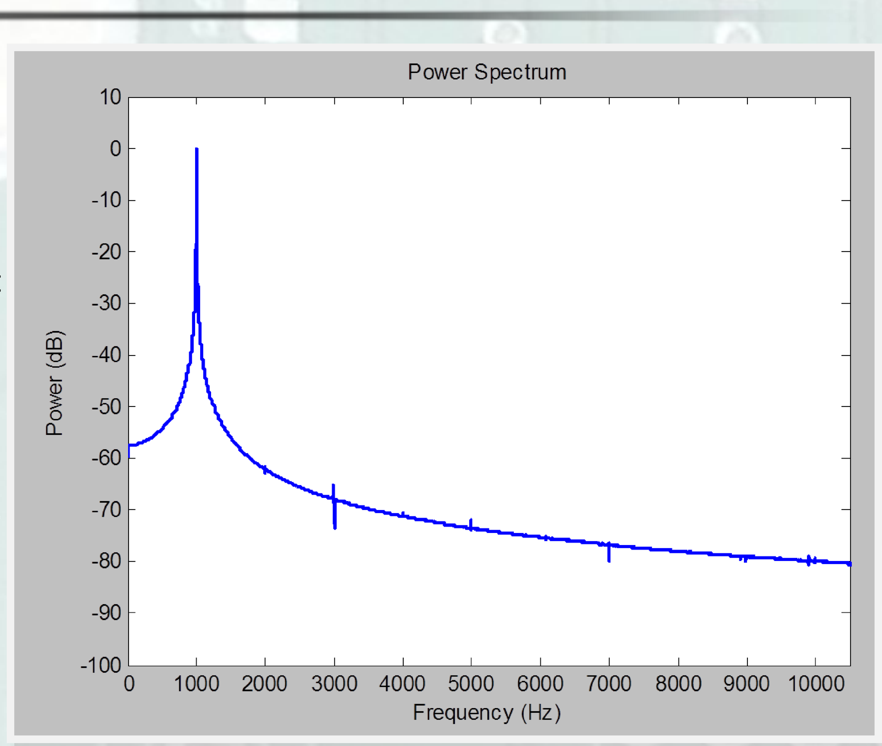
Traditional Test Method

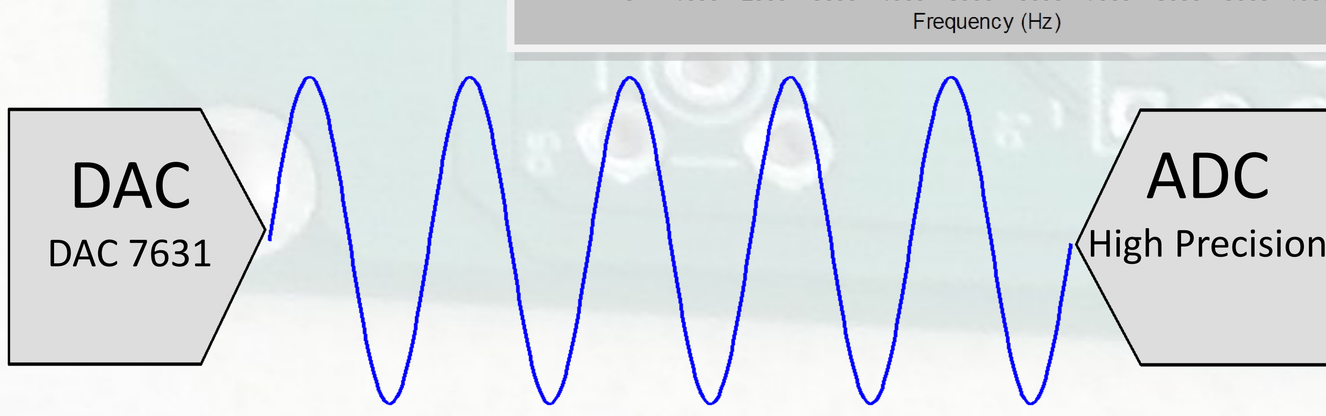
Traditional ADC test method: requires a high precision wave generator, or a higher precision DAC (costly and time consuming). The new test board was able to collect the power spectrum to the right. Coherent sampling was not made possible on this board for this specific test. This is not an issue since it has been shown that accurate spectral testing can still be found without coherency [1].



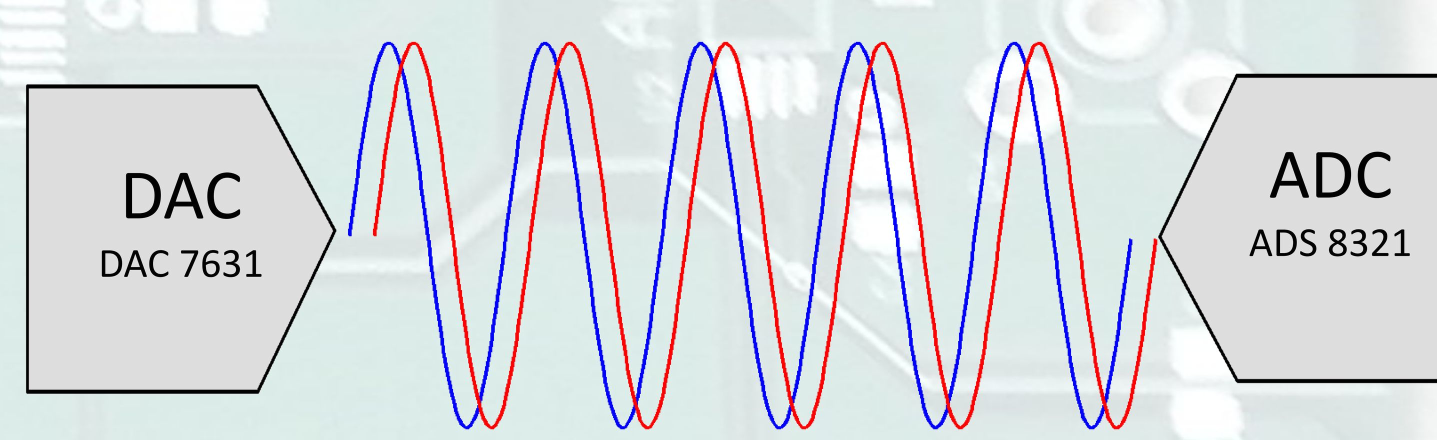


Traditional DAC test method: requires a higher precision ADC (costly and time consuming). The new test board was able to collect the power spectrum to the right. Again the board was not made to collect this data coherently, which will not be a problem as coherency is not required in order to have accurate results.



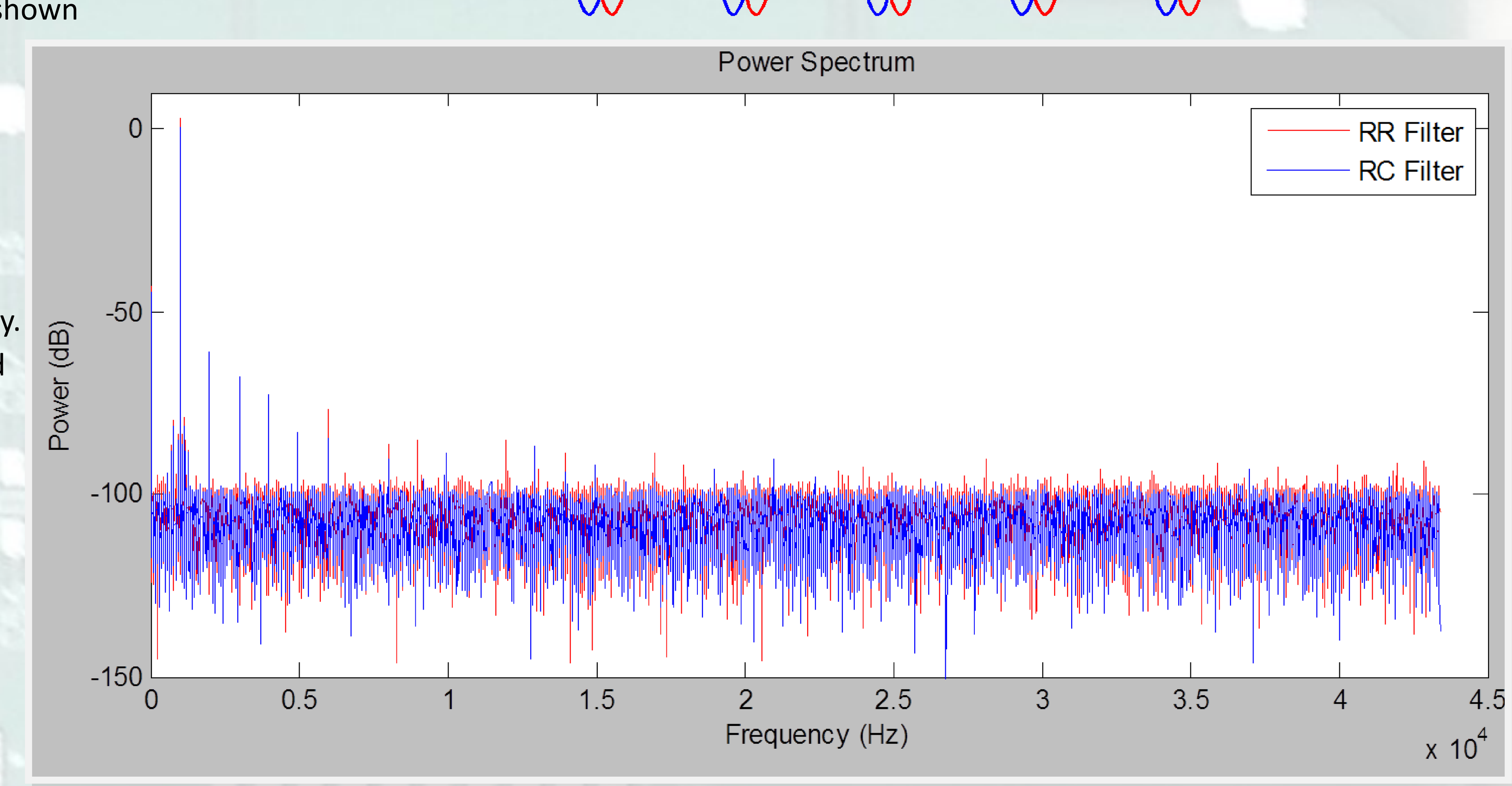


New Test Method & Results



NEW DAC / ADC test method; using a DAC / ADC pair (equal resolution). The DAC produces a sinusoidal wave that passes through two unique filters. Both filters have the same magnitude response at the fundamental frequency, but are different throughout the rest of the spectrum. The newly acquired power spectrum is shown below.

Shown in blue is the power spectrum of the signal through the RC filter and the red is of the signal through the RR filter. The spectrum clearly shows the harmonics of the fundamental frequency. This data and information can be passed to analysis algorithms and then compared to the traditional test methods; also obtained from the board.



The project met all requirements. The total cost of the project was around $183.00; a very low cost and efficient solution. A summary of the cost and of each product of this project is shown to the right. Each summary has a list of the tools used including parts, simulation software, and hardware instruments.

Cost [$]		Tools Used
PCB manufacture	$33.00	Advanced Circuits, Aurora CO
Parts	$150.00	TX Instruments / Analog Devices
FPGA	$0.00	Altera Cyclone II DE2
Precision tools	$0.00	Audio Precision/ 24b ADC evm.
total project cost	$183.00	

The board successfully generated and captured sinusoidal signals in addition to replicating current test methods. The primary difference being the required test time, the overall test cost, and the fact that all analysis and processing is purely digital. With this new test method, coherent sampling is very easy to attain. This project will be of great benefit to future research at Iowa State related to advanced testing methods of data converters and is supported by Texas Instruments. This project is also entered in the Texas Instruments senior design contest.

Product	Tools Used
PCB design	TINA - TI
PCB layout	Altium
FPGA/ Verilog prog.	Quartus II / Bench equipment
Matlab GUI	Matlab
Soldered PCB	Solder iron
PCB debug	Bench equipment

Future work on the project will focus on increasing the signal integrity on the board, decreasing any undesired non-idealities, and expanding to various data converter pairs. It will ultimately be used for data collection and verification of co-testing algorithms.

[1] S. Sudani, M. Wu, D. Chen, "A Novel and Accurate Spectral Testing Method for Non-coherent Sampling", IEEE International Test Conference, 2011, pp. 1-10

For more information please refer to the project website at: http://seniord.ece.iastate.edu/may1328

April 23, 2013