EE 432 Mask Fabrication
May 2013 – Group 25

Introduction

Microelectronics is a field in electrical engineering. EE 432 is a class offered at Iowa State University that teaches students more about the fabrication process in the modern world.

In this class, you will learn several modern integrated circuit fabrication processes. One of the processes, photolithography, is related to the senior design project that our group is involved in.

The professor of EE 432 has tasked our senior design group with improving the photolithography masks used in the EE 432 lab. The new photolithography design will be easier to align, more likely to create functional devices, and will use the wafer space more efficiently.

The old masks set had several small areas in which they can be improved. The contacts between mask and silicon wafer were not always reliable and the mask aligning was inefficient. It was providing very low yield when testing the devices.

The goal is to create new and better masks that are more reliable and easier to use.

Requirements

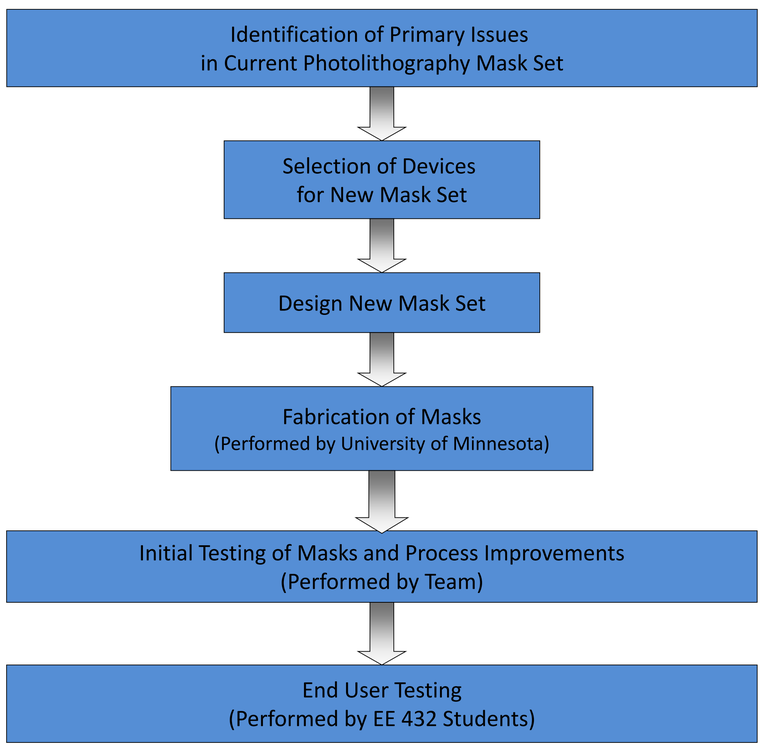
Functional Requirements:

1. Able to produce higher yielding wafers in comparison to previous masks set
2. Improve the contacts on the devices which will increase the yield when testing the devices
3. Improve the alignment marks and allow more room for human error

Non Functional Requirements

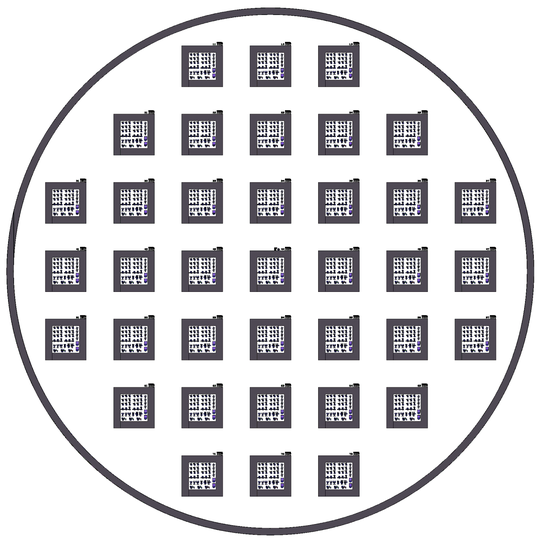
1. Consistent sizing and spacing of devices should follow design rules

Design Approach



Design Overview

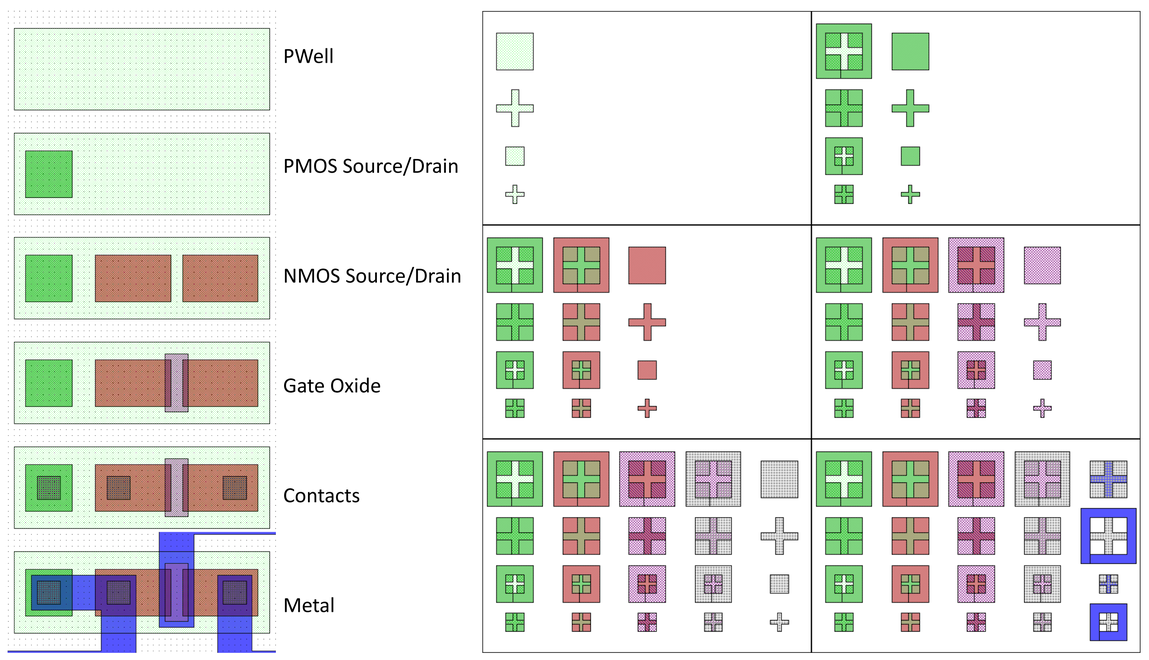
- Designed using Tanner L-Edit Software
- The mask set has 37 dies
- Each die contains 39 different devices
  - 24 MOSFETs
  - 3 BJTs
  - 4 TLM Test Patterns
  - 3 Van der Pauw Test Patterns
  - 2 MOS Capacitors
  - 3 Logic Gates
- The MOSFET feature size ranges from $L = 5\mu m$ to $L = 20\mu m$
- There is a set of alignment marks in the upper right corner of each die
- We added a ring around all the dies that allows for easier alignment to the mask aligner



Test Plan

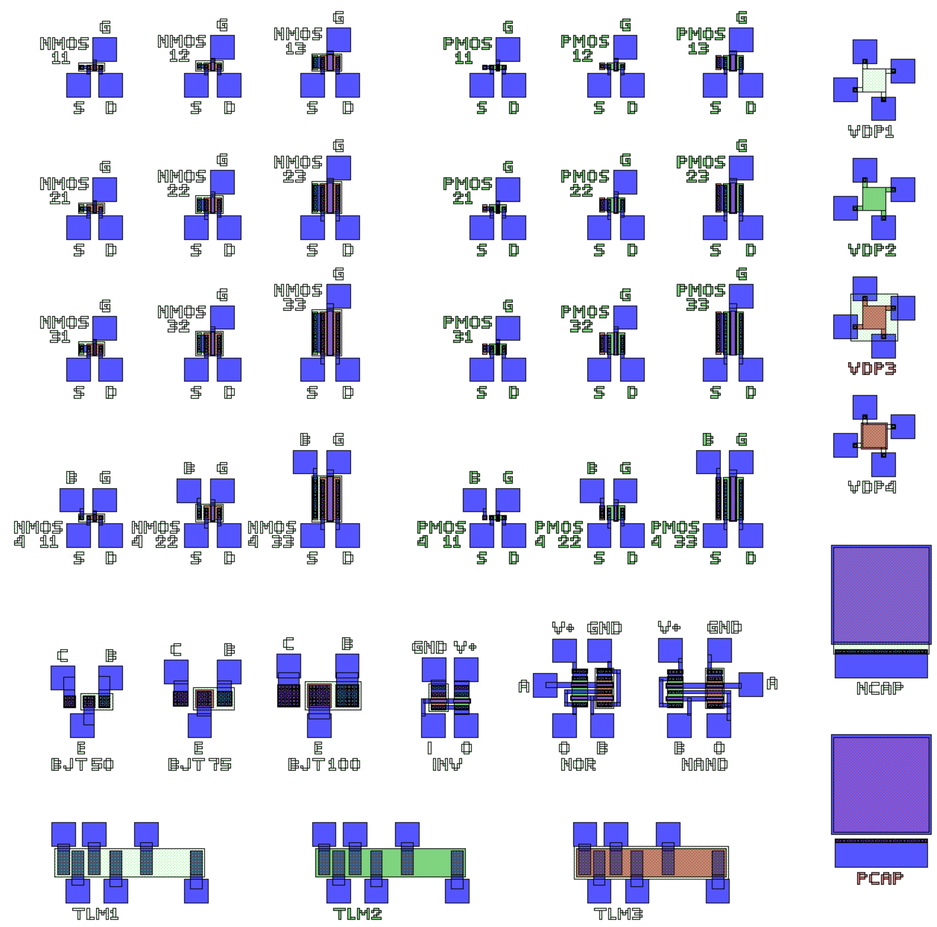
- Initial design was analyzed by each member of the group, as well as the advisor, before fabrication.
- After fabrication, the mask set was used in the spring semester of the EE432. Feedback was given by students on the usability of the new alignment marks.
- At the end of the semester wafers from each group will be tested.
- Tests will include MOSFET testing, contact testing, and capacitance measurements.
- Device yields will be calculated and low yielding devices will be further analyzed.

Transistor/Alignment Mark Design



Left: A walkthrough of the steps to build a single NMOS Transistor. Each step represents one mask.
Right: Each box represents what the alignment area looks like after each mask.

Die Design



Conclusion

The overall goal of this project was to improve the masks set for EE 432 in order to obtain better yielding working devices and increase the overall teaching effectiveness. This will allow student to be able to understand how the devices work when the results are accurate.

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