EE 491 Photolithography Mask

Project Plan

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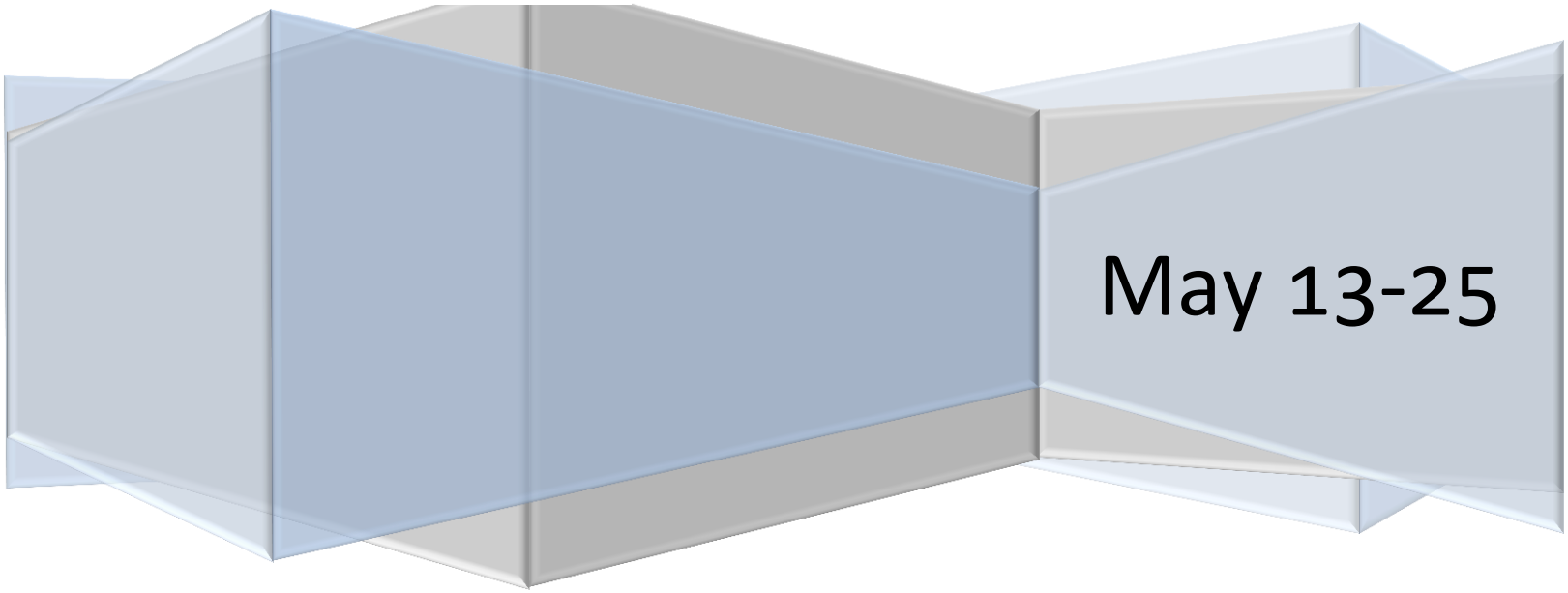


Table of Contents

Definitions

- Photolithography: A process used in micro-fabrication to selectively remove parts silicon dioxide from small areas of a wafer.
- Photoresist: A polymer that is weakened by UV light touching it. After exposure the weakened areas can be removed using a developer solution.
- Silicon Wafer: A thin slice of semiconductor material, such as a silicon crystal, used in the fabrication of integrated circuits and other micro-devices
- MOSFET: A transistor used for amplifying or switching electronic signals
- PMOS/NMOS: MOSFETS that have either electrons or holes that are carried through the channel of the MOSFET
- P-well/N-well: A layer of the MOSFET
- Alignment: The process in which the photolithography mask is placed and rearranged on the wafer so the transistors on the mask and wafer line up
- MRC: Microelectronics Research Center at Iowa State University

Problem Statement

The photolithography masks for EE432 are getting old and need to be replaced. Our team tasked with creating a design for new masks. The old masks had several small areas in which they can be improved. The contacts between mask and silicon wafer were not always reliable and the mask aligning was inefficient. The goal is to create new and better masks that are more reliable and easier to use.

Background Information

Microelectronics is a field in electrical engineering. EE 432 is a class offered at Iowa State University that teaches students more about the semiconductor fabrication process in the modern world. The lab for this class has students complete a very simple CMOS process over 10 four hour labs.

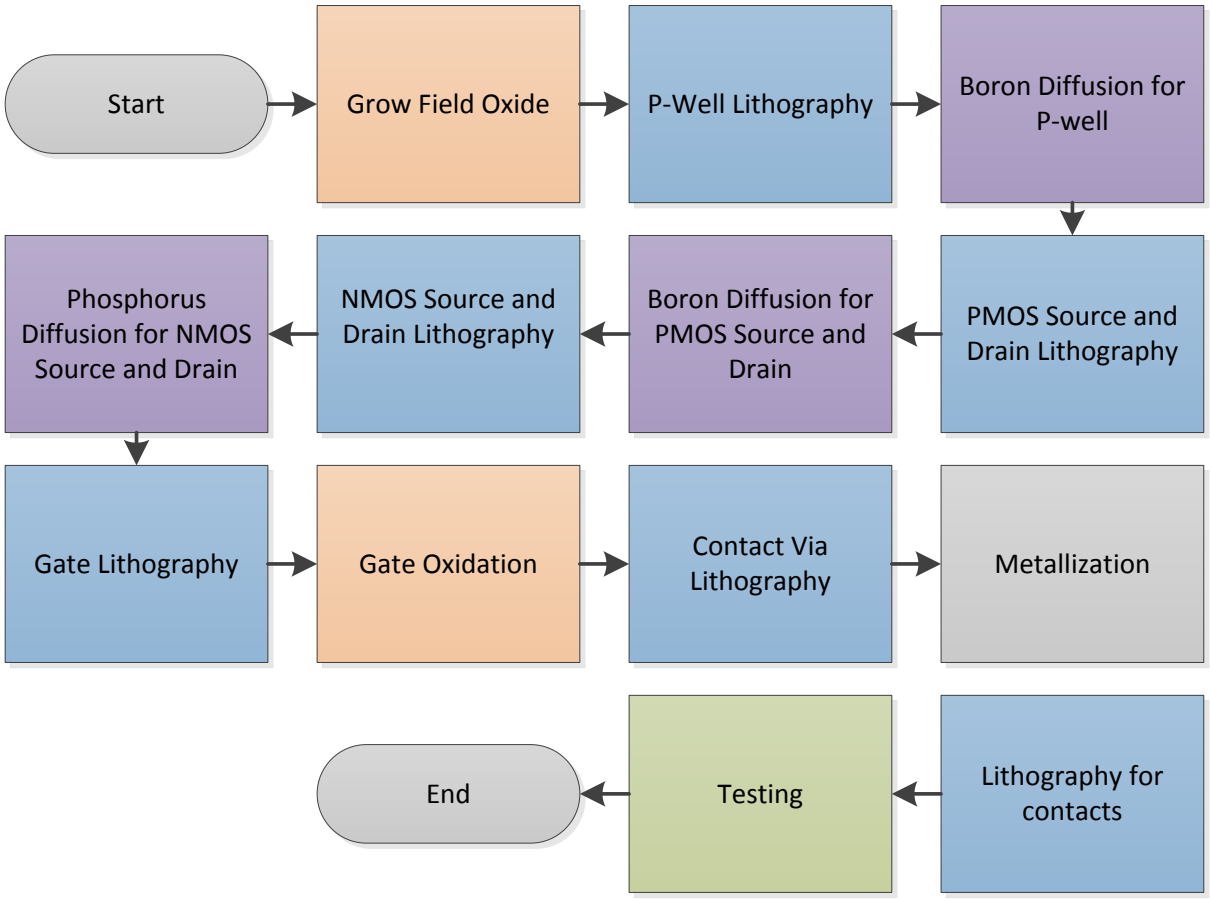


Figure 1: Overview of the CMOS process at ISU

The steps we are interested in improving are the lithography steps. Each lithography step requires a different mask. The process will take six masks in total.

The steps for photolithography are outlined below:

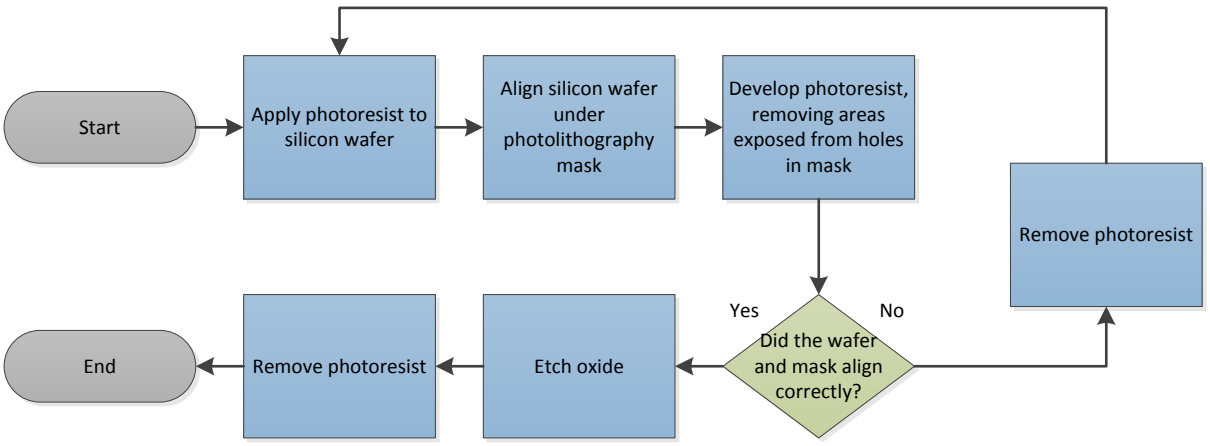


Figure 2: A flow chart of the photolithography process

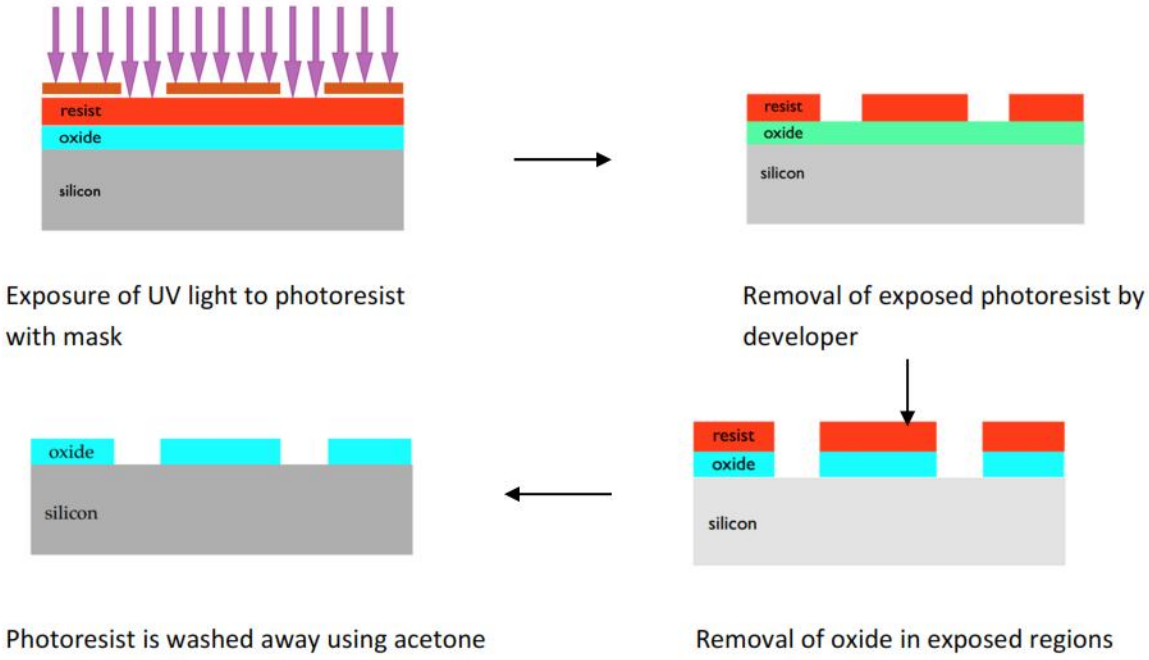


Figure 3: An overview of the photolithography process.

One of the steps we are interested in improving is the alignment step. The newly designed masked will be easier to align and will be more forgiving if misalignment occurs.

Concept Sketch

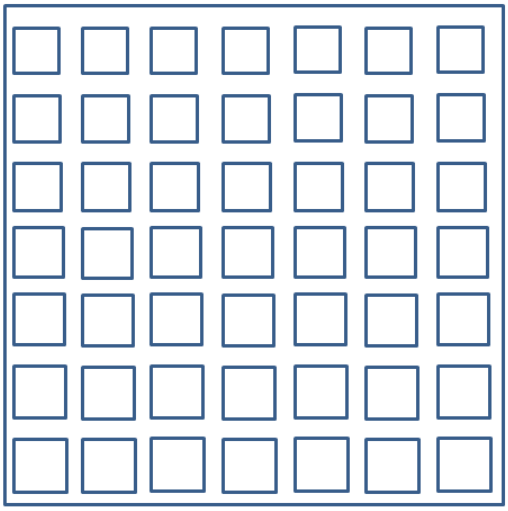


Figure 5: A single die layout. Each square represents one device.

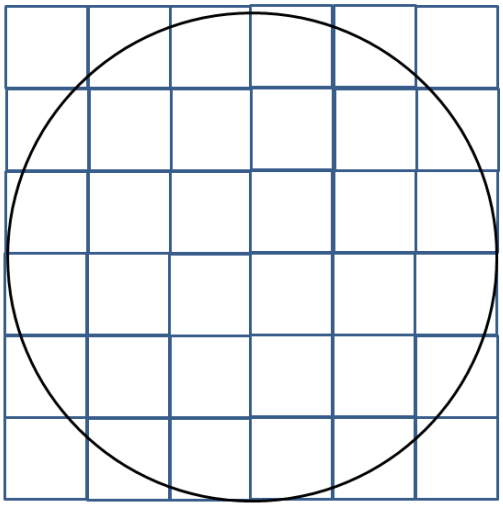


Figure 4: The entire mask layout. Each square is one die.

Requirements

Functional Requirements

- Produce a set of masks that can be used in the EE 432 lab process
- Must have an alignment system

Non-Functional Requirements

- Allow for easier alignment
- Larger contact vias to increase the chance of forming good contacts
- Add more space between contacts and wells to allow for greater margin of error while aligning the mask
- Simple design for cost effective mask fabrication

Resource Requirements

There are several resources needed:

- Software - L edit. This software will allow us to create the mask pattern and the devices on the mask. This costs about $300 for a license for one year.

- Mask fabrication machine - After finalizing our mask pattern, the mask will be fabricated using this machine that is in the MRC.
- Mask fabrication machine in other institutions - If the one in MRC does not work. Masks cost about $280 per mask if done at the University of Minnesota.
- Silicon Wafers – These will be used to test our design. They cost about $10 per wafer.
- Chemicals used in processing wafers – These will be provided at the MRC.

Deliverables

- Six photolithography masks that work with the current process at the MRC.
- One batch of silicon wafers that have gone through the entire 432 lab process using the new masks
- Documentation of the masks
- Final report and presentation

Risks

We need to ensure that the mask fabrication machine at the MRC is functional. Otherwise, our client, Gary Tuttle will have to supply more money in order to get the mask fabricated at University of Minnesota, Twin Cities. If that fails, more money will have to be supplied to send the mask to be fabricated in other institutions in California.

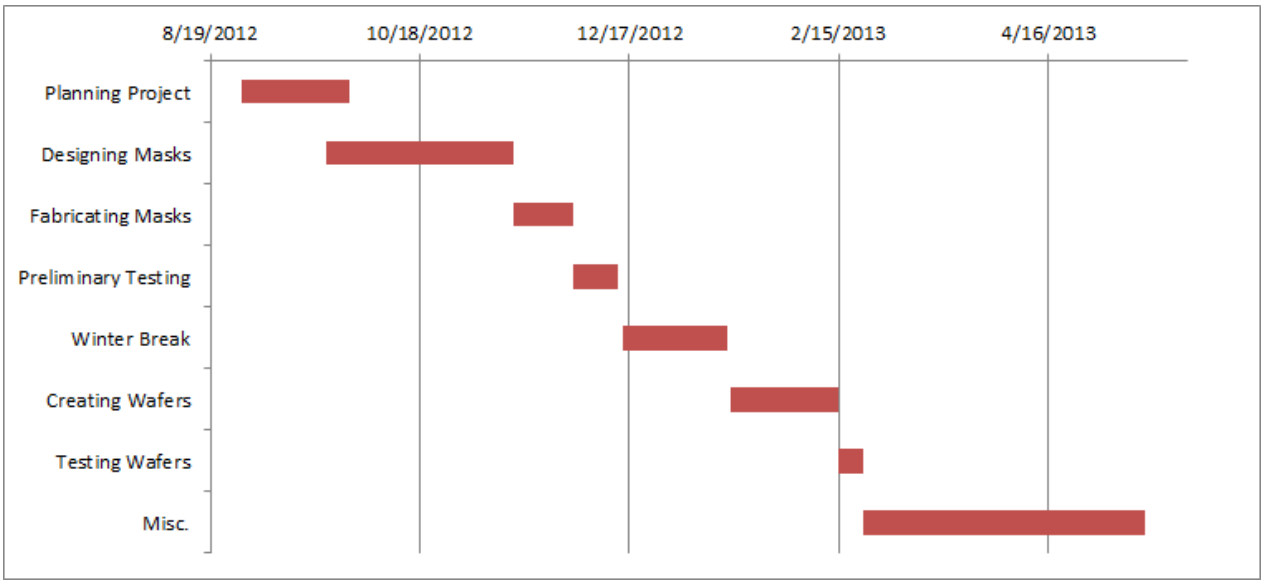
Our client might need to use the old mask if the new fabricated mask fails to function as well or better than its predecessor, or if they are not created before the spring semester.

Mitigation

We will do several checks before we send the design to be fabricated. We only want to have to pay for one set of masks so we will need to be sure the design is correct before we order the masks.

Schedule

Gantt Chart



Milestones

- Decide on device sizes – Completed
- Designing template transistor in L-Edit – Completed
- Design all devices that will be included in the design – In progress
- Fabricate mask set
- Run at least one set of wafers through the CyMOS process.
- Test the wafers