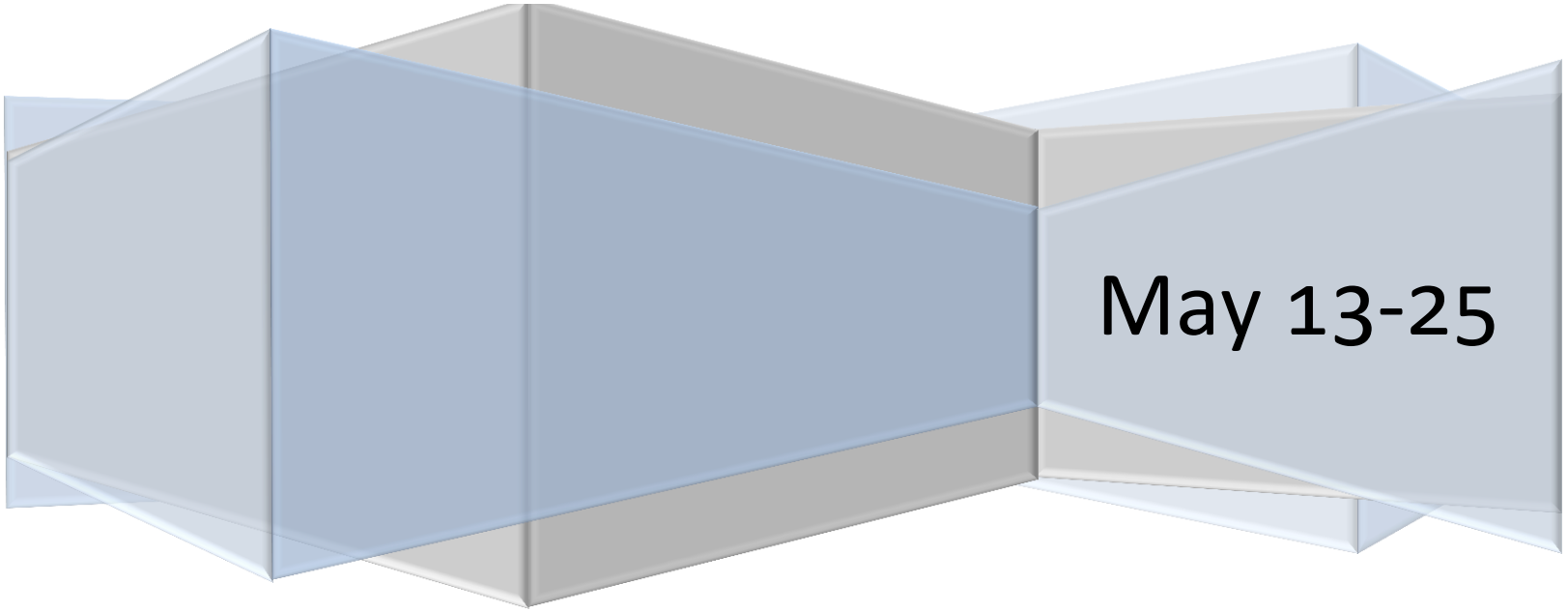
EE 491 Photolithography Mask

Design Document

Client: Dr. Gary Tuttle
Advisor: Dr. Gary Tuttle

Daniel O'Connell
Levi Weiss
Benjamin Ch'ng
Chen Wen
Wang Liao



Contents

Executive Summary

Introduction

Microelectronics is a field in electrical engineering. EE 432 is a class offered at Iowa State University that teaches students more about the fabrication process in the modern world. In this class, you will learn several modern integrated circuit fabrication processes. One of the processes, photolithography, is related to the senior design project that our group is involved in.

The professor of EE 432 has tasked our senior design group with improving the photolithography masks used in the EE 432 lab. The new photolithography design will be easier to align, more likely to create functional devices, and will use the wafer space more efficiently.

We will use L-edit software to design the new photolithography mask. After the design is finalized, we will send the design to the University of Minnesota to be fabricated.

Scope

The scope of the project is limited the design of the photolithography masks for the CMOS process used in EE 432. Other significant changes to the process are outside the scope of this project. Our masks must work with the process as is, with no changes.

Members

Daniel O'Connell	Team Leader
Levi Weiss	Communications Liaison
Benjamin Ch'ng	Webmaster
Chen Wen	Design Engineer
Wang Liao	Design Engineer

Problem Statement

The photolithography masks for EE432 are getting old and need to be replaced. Our team is tasked with creating a design for new masks. The old masks have several small areas in which they can be improved. The contacts between mask and silicon wafer are not always reliable and the mask aligning is inefficient. Professor Tuttle, our client, has decided to replace the old masks. The goal is to create new and better masks that are more reliable and easier to use.

EE432 Definition

EE 432 is a senior tech elective class that focuses on the microelectronics field. It is also known as Microelectronics Fabrication Techniques class. In the lab portion of the class, students are exposed to the techniques used in modern integrated circuit fabrication, including diffusion, oxidation, ion implantation, photolithography, evaporation, sputtering, chemical-vapor deposition, and etching.

Our senior design project is focused on improving the masks used in photolithography. Photolithography requires the use of patterned, square glass masks that cover the silicon wafer when it is exposed to UV light. The areas of the wafer that the mask covered will not be removed when the wafers are etched. This will pattern different devices on the silicon wafer.

System Design

Functional decomposition

The overall function of this mask is crucial in the silicon fabrication process. The mask will be utilized during photolithography. The mask will be placed between the silicon wafer and a microscope. The mask and the silicon wafer are then aligned. After alignment, the wafer and mask are exposed to UV light. The mask will block light in specific areas on the wafer, and therefore allows a particular section of the device areas to be patterned. After several masks are used, the entire design for the device will be made.

System analysis

There are no sub functions of the mask. The only function the mask has is to block UV light to put patterns on the silicon wafer.

System Requirements

Education

The photolithography masks will be used in an undergraduate lab to teach about semiconductor processes. The design is limited by the equipment available in the lab. As such, we will be making no changes to the actual process. The design should be understandable and usable by undergraduate students.

Working devices

In previous semesters the yield rate for devices on some batches approached 0%. We believe this may be a result of a design that is too aggressive. Going through the process is still useful for students if the

devices don't function, but it will be more useful if the students get to test working devices. The main device we would like to be functional is the MOSFET.

Better Contacts

An improvement that can be made of the old mask set is the size of the contacts. The old contacts are 5um by 5um. These turned out as circles when used during photolithography. The contacts sometimes would not conduct well. We will be increasing these 10um by 10um which should guarantee working contacts close to 100 percent of the time.

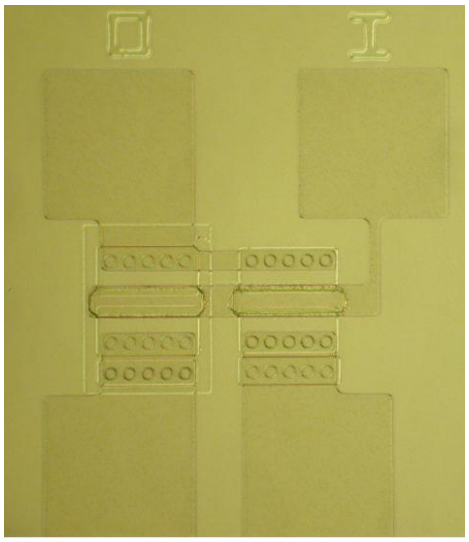


Figure 1: An inverter showing the contacts turned out as circles

More Overlaps

The current masks use very little overlap between layers. This is a good thing in industry where alignment of different layers can be done very consistently. In the lab alignment is done by students who have only aligned masks one or two times. We are going to increase the overlaps between layers so that there is more margin of error when aligning the mask layers. This has two downsides; it increases area and parasitic capacitances. This means our devices will operate at a slower speed. This is not a major concern for our design because we have single devices that will be used for education only.

More Spacing

The current design has a lot of unused space but the devices are still packed very close together. We are going to increase spacing between devices while keeping the same number of devices. This will allow more area to add alignment marks between dies which we talk about in the next section.

Alignment marks

The current alignment marks work but can be improved. The major improvement we would like to make is to increase the amount of alignment marks on the mask. There are currently four alignment marks per mask. We are going to increase that number to one per die. This will allow the masks to be aligned more quickly.

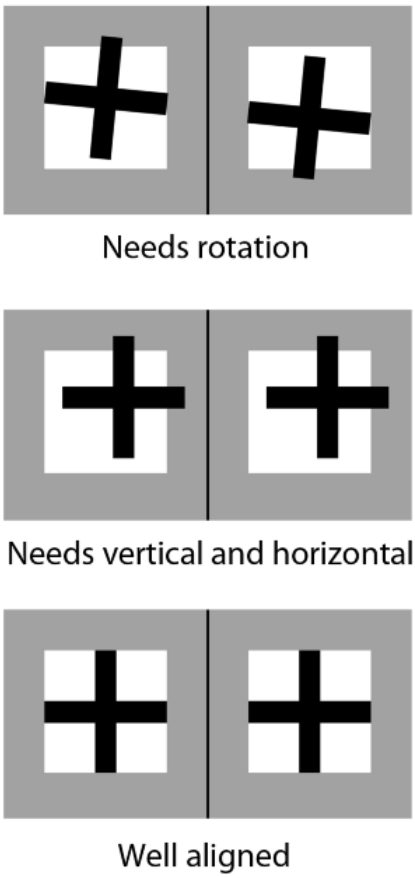


Figure 2: Example alignment marks

Standards

Design Rules

When designing devices for a particular semiconductor process a set of rules is used to determine the minimum spacing of layers. These are usually defined after many tests are performed on the process. For our process we do not have the resources to find the absolute minimum spacings. Instead we chose to define conservative estimates based on analysis. The most important objective is that the final product works and not that it is minimum sized. The major downsides to having less aggressive design rules are more area, and more parasitic capacitances. Neither of these are a big concern because we will be using the masks in a learning environment.

Detail Design

Input/output specification

Input: UV light, mask and silicon wafer.

Output: a patterned silicon wafer with different devices patterned and ready for testing.

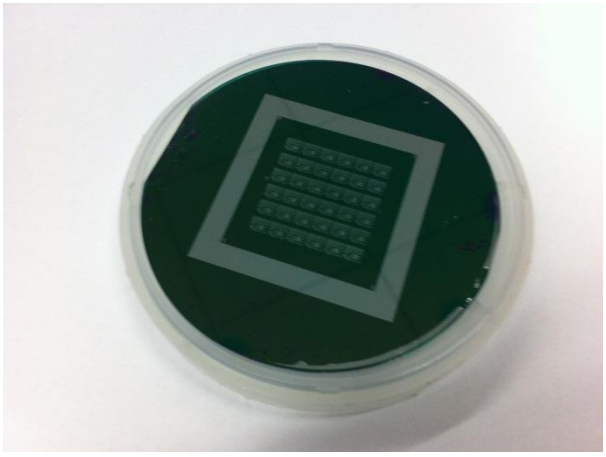


Figure 3: A finished silicon wafer that has been run through the CyMOS process

User interface specification

The user will interact with the mask using a mask alignment machine. This machine consists of a microscope and dials to make fine adjustments of position to the wafer. The user will look through the microscope and find alignment marks. They will then need to align this mark on the mask with the corresponding mark on the wafer. Once aligned, the machine will shine UV light through the mask.

Hardware and/or software specifications

First we will need a software program called L-edit to design the mask. After finalizing the mask design, we will need a stepper to fabricate the mask. A stepper is a machine used to pattern the transparent or opaque areas on the mask. The software was acquired by our client. There is a stepper available for use at Iowa State University, but it may not be in working order. If the stepper will not work we will send the design to another facility to be fabricated.

Test plan

We will test the mask set in the microelectronics research center. The tests will be run in the first weeks of the spring semester. The tests will give the spring EE 432 class a pre-evaluation of their class materials. These tests will be used to test the efficiency and improvement made since the old mask set was used.

A test batch of 10 wafers will be used for the process. The wafers will be run through the entire EE 432 process using the new mask set. After the silicon wafer has gone through the EE 432 process, the wafer will be analyzed to see if the components function correctly. The success of the mask set depends on the percent of functional devices as well as the ease of alignment.

Simulation, modeling and/or prototyping

Modeling and analysis of the system will be done by hand. Analysis will need to confirm that devices are spaced far enough apart to function properly. After analyzing one device the spacing can be generalized to devices of other size

CAD Design

The final mask set will be designed using a CAD tool called L-Edit. We have begun designing using L-Edit and have most of the transistors laid out. Below we have an example of a BJT and an NMOS. They are both to scale. The MOSFET and BJT drawings are the smallest we will implement of either. The spacing will remain constant but the size and amount of contacts will increase.

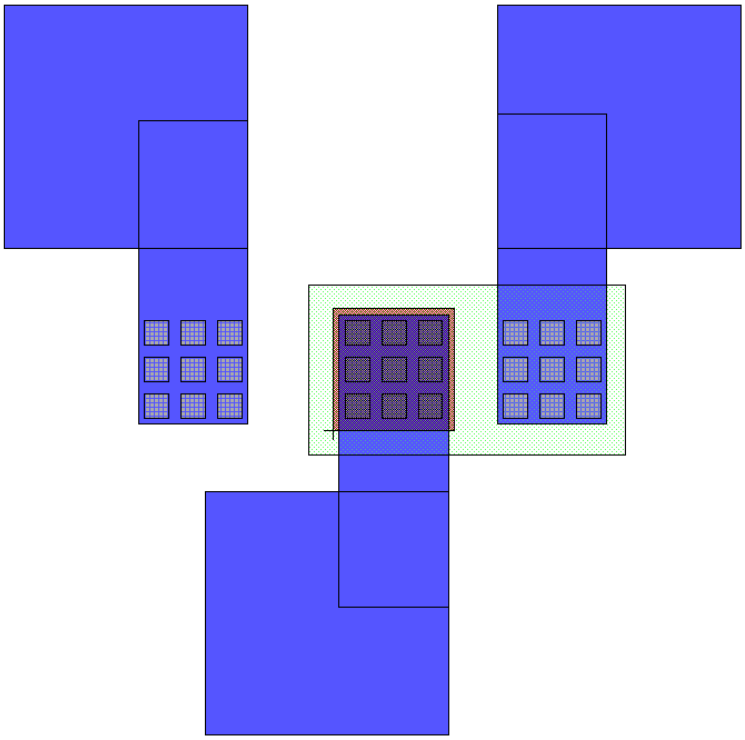


Figure 4: A layout- of a BJT with Ae = 50um x 50um

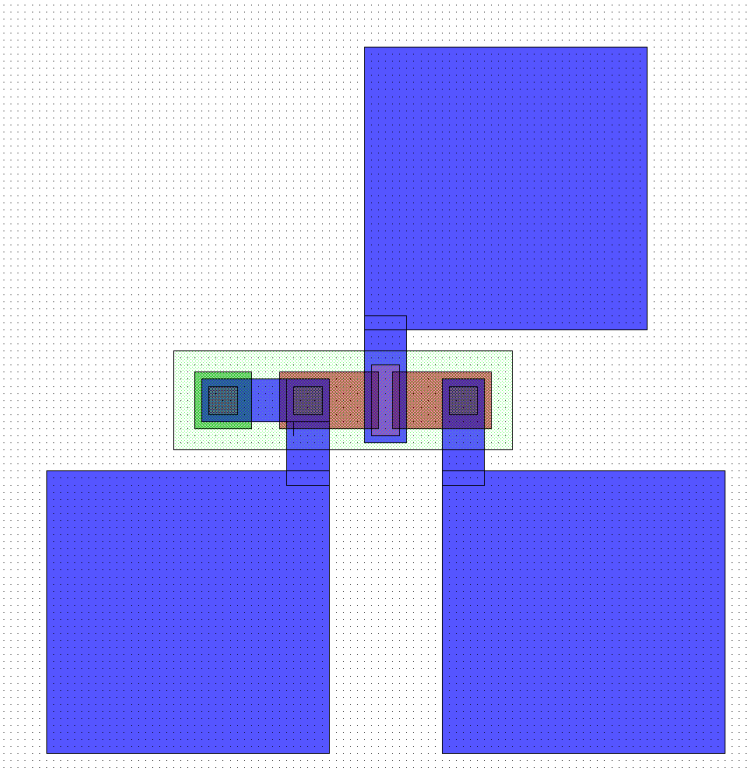


Figure 5: A layout of an NMOS with W = 20um and L = 5um

Risk and Issues

We need to ensure that the mask fabrication machine at the MRC is functional. Otherwise, our client, Gary Tuttle will have to supply more money in order to get the mask fabricated at University of Minnesota, Twin Cities. If that fails, more money will have to be supplied to send the mask to be fabricated in other institutions in California.

Our client might need to use the old mask if the new fabricated mask fails to function as well or better than its predecessor, or if they are not created before the spring semester.

Appendix

Devices On Each Die

Devices per Die	Amount
NMOS (3 Terminal)	9
PMOS (3 Terminal)	9
NMOS (4 Terminal)	3
PMOS (4 Terminal)	3
BJTs (NPN)	3
Diodes	3
TLM Test Patterns	3
VDP Test Patterns	3
NMOS Cap	2
PMOS Cap	2
Inverter	1
NAND	1
NOR	1

Sizing of MOSFETs

All Sizes are in microns

Constants	
Contact Size	10
Metal Width	15
Metal Spacing	10

	L	W
Channel	5	15
Gate Oxide	10	20
Source and Drain	30	15
Bulk	15	15
Well	100	30
Number of Contacts	1	

	L	W
Channel	10	30
Gate Oxide	15	35
Source and Drain	30	30
Bulk	15	30
Well	105	45
Number of Contacts	2	

	L	W
Channel	20	60
Gate Oxide	25	65
Source and Drain	30	60
Bulk	15	60
Well	115	75
Number of Contacts	4	

	L	W
Channel	5	30
Gate Oxide	10	35
Source and Drain	30	30
Bulk	15	30
Well	100	45
Number of Contacts	2	

	L	W
Channel	10	60
Gate Oxide	15	65
Source and Drain	30	60
Bulk	15	60
Well	105	75
Number of Contacts	4	

	L	W
Channel	20	120
Gate Oxide	25	125
Source and Drain	30	120
Bulk	15	120
Well	115	135
Number of Contacts	8	

	L	W
Channel	5	45
Gate Oxide	10	50
Source and Drain	30	45
Bulk	15	45
Well	100	60
Number of Contacts	3	

	L	W
Channel	10	90
Gate Oxide	15	95
Source and Drain	30	90
Bulk	15	90
Well	105	105
Number of Contacts	6	

	L	W
Channel	20	180
Gate Oxide	25	185
Source and Drain	30	180
Bulk	15	180
Well	115	195
Number of Contacts	12	