Device Interface Board Design for Wireless LAN Testing

Design Report

Team
May 05-29

Client
ECpE Department

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List of Definitions

ASK modulation – Amplitude shift keying. In this modulation scheme the amplitude is varied to indicate logic 0's and 1's

BASIC – Beginners All-Purpose Symbolic Instruction Code. A simple programming language used in the IG-XL software

Coover Hall – The electrical engineering building on the Iowa State campus that houses the Teradyne J750

ESD – Electrostatic discharge, or simply the discharge of static electricity

ECpE – Electrical and Computer Engineering

DIB – Device interface board. This board is the physical interface between the Teradyne and chip attached to the Teradyne

D flip-flop – A circuit diagram for a D flip-flop is shown in Figure 1 below. The operation of a D flip-flop is that when the clock input falls to logic 0 the Q output always takes on the state of the D input at the moment of the clock edge.

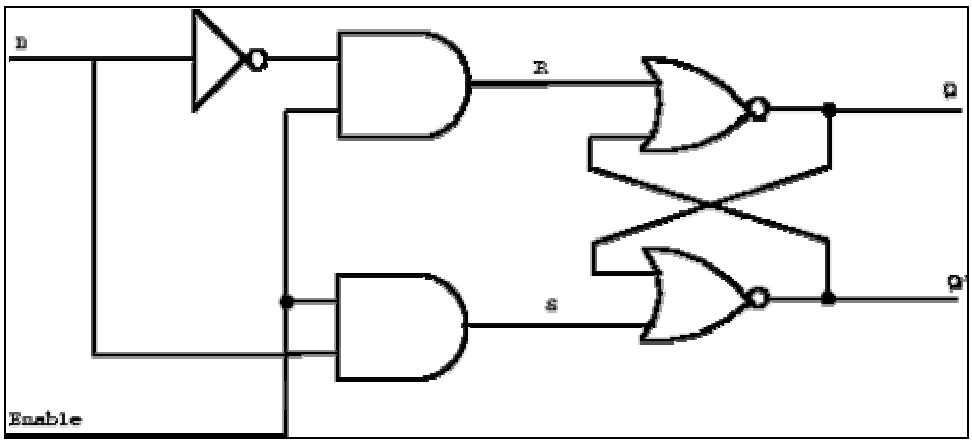

Figure 1: Gate level implementation of a D flip-flop

DUT – Device under test. In this paper, it refers to any wireless chip that could be tested by the Teradyne

DRAM – Dynamic random access memory – a type of memory that needs to be refreshed every few milliseconds.

ESD – Electrostatic discharge. Commonly called static electricity.

FPGA – Field programmable gate array

Half-duplex - Half-duplex data transmission means that data can be transmitted in both directions (send and receive) on a signal carrier, but not at the same time.

Header – Bits that are placed in front of actual data and are usually repeated as a standard part of the units of data transmission

IG-XL – Software package used to develop test programs for the Teradyne J750

ISU – Iowa State University

I/O – Input and output

Kbps – Kilo-bits per second, or 1000 bits per second.
LAN – Local area network
Milling machine – A machine used to create printed circuit boards
Mbps – Mega-bits per second, or 1000000 bits per second.
Packet – A packet is the unit of data that is routed between an origin and a destination
PC – Personal Computer
PCB – Printed circuit board. Refers to any circuit fabricated on a dielectric board – ubiquitous in the electronics industry.
PLL – Phase-locked loop (Refer to Appendix B for operation).
RF – Radio frequency, refers to signals with frequency in the 9kHz-300Ghz range
RFM – Radio Frequency Monolithics. A company that sells radio frequency components.
Shift register – A device that shifts in or out data according to its operation (parallel to serial or serial to parallel)
SNR – Signal-to-noise ratio.
S/R network – Send and receive network. In this paper, it is used to refer to the entire wireless network that will be implemented as a result of the project.
Teradyne J750 – Tester donated to Iowa State University by Teradyne. Seen below, it is used in the testing of printed circuit boards and integrated circuits.

Figure 2: Teradyne J750

TDR – Time domain reflectometry. This refers to making paths that signals take in the time domain equal so the signals arrive at the same time.
TRM1, TRM2, RCV1, RCV2 – TRM1 and RCV1 are the wireless transmitter and receiver units on the input side of the network, respectively. TRM2 and RCV2 are the wireless transmitter and receiver units on the output side of the network, respectively.

1. Introductory Material

This section will introduce the project, including the abstract, acknowledgements, problem statement and solution, operating environment, intended users and uses, limitations and assumptions, expected end product and other deliverables

1.1 Executive Summary

Introduction

Today, hundreds of companies are producing wireless LAN cards and routers. These wireless products must be tested to ensure that they perform as desired. The Department of Electrical and Computer Engineering at Iowa State would like to use the Teradyne J750 to test the RF components of wireless chips, but there is currently no way to do so. The purpose of this project is to investigate the feasibility of a send/receive network through which the J750 can wirelessly test devices. An executive summary of the report regarding the send/receive network that will be developed is below.

Introductory Materials

In this section the team will discuss the operating environment, intended users and uses, assumptions and limitations, expected end-product.

Operating Environment

The Teradyne J750 is located in Coover Hall, the electrical and computer engineering building at Iowa State University. The send/receive network that the project will implement will also operate within Coover Hall. Further, the J750 can only operate from 27°C to 33°C, so the send/receive network will not endure any temperatures outside that range. Finally, the J750 is very sensitive to electrical shock - as a result, everyone who uses the J750 must wear an electrostatic discharge band while using it. So, the send/receive network will not be exposed to any electrostatic discharge.

Intended Users and Uses

The intended users of the send/receive network are members of the Department of Electrical and Computer Engineering that need to wirelessly test components using the Teradyne J750. The size and sex of the person don't have any bearing on their ability to test, however they must posses a basic knowledge of RF communication and understand how to set up and run a test on the J750.

The intended use of the system is to allow the J750 to wirelessly send inputs to a single device under test, make the device under test accept the inputs and wirelessly send the outputs from the device under test back to the J750.

Assumptions and Limitations

The following are the most important assumptions the team has made:

- User can set up and execute a test on the J750
- User has knowledge of inputs and outputs of device under test

- Maximum data rate at which the user can send data is 115.2 Kbps

The following are the most important limitations of the wireless system:

- Devices under test must be digital
- The operating environment must be between 27°C and 33°C
- The Teradyne J750 has not been calibrated since 2003

Expected End-Product

The team expects to produce a solid feasibility study into the send/receive network that will allow the J750 to send inputs to a remote device under test and wirelessly receive the outputs from the device under test. Once the system is developed to test one device, a demonstration of that test and a manual will be created for future users to configure their own wireless tests. If the system is unsuccessful, the results will be given to Teradyne for their consideration.

Approach and Design

In this section the team will discuss the design objectives, functional requirements, design constraints, technology considerations, testing and project continuation.

Approach Used

This section summarizes the different aspects of the approach used to design the send/receive network.

Design Objectives

The most important objectives of the design are:

- Develop an interface between the Teradyne J750 and the wireless input transmitter
- Develop an interface between the input transmitter and receiver and output transmitter and receiver
- Create a user manual for future users

Functional Requirements

The most important functional requirements of the end product are:

- Successful data transmission from Teradyne J750 to wireless transmitter
- Strong communication link between input and output transmitters and receivers
- No interference between the two wireless connections
- Successful data transmission from receiver to device under test
- Successful data transmission from device under test to output transmitter

Design Constraints

The design constraints listed below are results of the assumptions and limitations of the product.

- The system shall be limited to using only one frequency for each communication channel.

- The data transmission rate on the Teradyne J750 shall be slowed to accommodate the slower wireless data rate.
- The distance between the receivers and transmitters is limited to 5 feet.
- The operating conditions are limited to 30°C ± 3°C.
- The budget for the project is limited to $150.00
- The Teradyne lab is only accessible by selected faculty and students.
- The system shall only use one field programmable gate-array.

Technology Considerations

Various technologies were considered for the parallel to serial data converter, wireless communication system, serial to parallel data converter, language for the FPGA and clock recovery circuit.

The technologies chosen for each subsystem respectively are:

- Shift register
- Individual receiver and transmitter modules (900MHz)
- FPGA
- Verilog
- PLL

Testing

The end product will be tested thoroughly for full functionality. Each sub section will be tested individually concentrating mainly on the frequency of data transmission and latency issues. A test form has been created to facilitate the testing of each subsection.

Project Continuation

The team recommends continuing the project as envisioned. Also the product could be improved by increasing distance between the tester and DUT and various other DUT's.

Detailed Design

The purpose of this section is to give an overview of the design that will be created. The send/receive system can be summarized using the block diagram shown in Figure 3

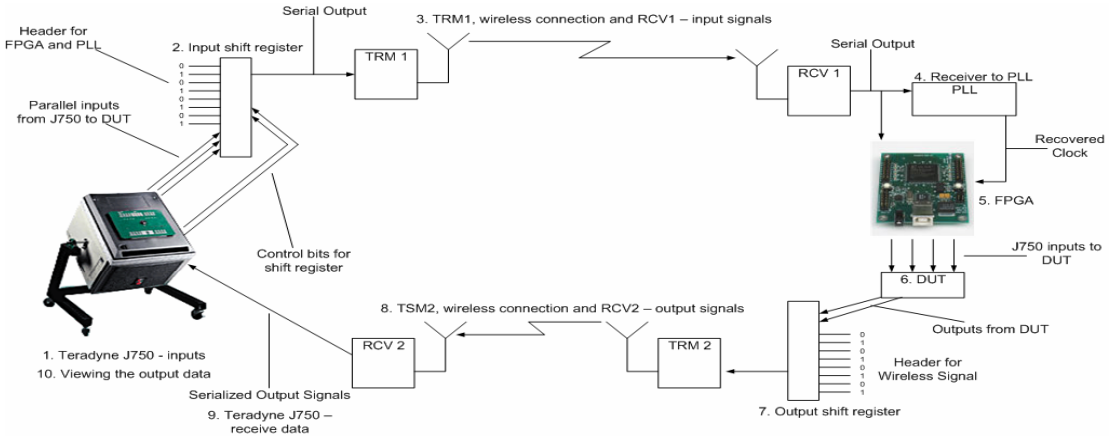

Figure 3: Summary of the send/receive network that will be implemented

The major subsystems of the design are numbered in Figure 3. The subsystems are also listed below with a brief description. For more information on any subsystem, refer to the corresponding section of the report.

1. **Teradyne J750 – inputs**. In order to test any device, the Teradyne J750 must be programmed to create the inputs that will test the device. The J750 must also generate the control signals to control the input shift register. In order to create an input signal, one must map the output of the J750 to a channel, define a clock period and program the values the input takes during each period.

2. **Input shift register**. The input shift register is controlled by the control signals from the Teradyne J750. It takes the parallel inputs from the J750 to the device under test and shifts them out in a serial stream. The register also attaches a pattern of 101010101010 before each data transmission to facilitate clock recovery on the DUT side of the system so that the transmission will be recognized by the FPGA.

3. **TRM1, wireless connection, and RCV1 – input signals**. TRM1 is the first wireless transmitter in the system. RCV1 is the first wireless receiver in the system. Together, TRM1 and RCV1 wirelessly transmit and receive the serialized data generated by the input shift register. They both operate at 916.5 MHz and transmit data at 115.2 Kbps.

4. **PLL**. PLL stands for phase-locked loop. A phase locked-loop takes data and attempts to recover the clock signal of the data. In this case, the PLL receives the wirelessly transmitted data from RCV1. The first set of data that it reads for every transmission is 101010101010 (the pattern attached by the input shift register). The rapid switching from 1 to 0 allows the PLL to recover the clock signal of the data, and it feeds the clock to the field-programmable gate array (FPGA) so that the FPGA can read the data at the correct rate.

5. **FPGA**. FPGA stands for field-programmable gate array. It is a chip that can be programmed to perform operations. In the send/receive network it is used to recognize the pattern 101010101010 that is sent prior to each set of inputs. When it sees the pattern, it reads the next four bits of data, which are those inputs sent to the device under test from the Teradyne J750. Once the FPGA has read the four input bits, it sends them simultaneously to the device under test – this is how the inputs from the J750 are delivered to the device under test.

6. **DUT**. DUT stands for device under test. The team has chosen a D flip-flop for the first DUT used in the send/receive network. The D flip-flop is a simple device, but its inputs and outputs are well understood, and it provides a good starting point from which the S/R network can be scaled to test larger devices.

7. **Output shift register**. The output shift register takes the parallel output signals from the DUT and serializes them so that they can be transmitted using TRM2. It

also attaches a pattern of 1's and 0's to the DUT outputs so that they can be easily viewed when they are received by the Teradyne J750.

8. **TRM2, wireless connection and RCV2 – output signals**. TRM2 is the second wireless transmitter in the system. RCV2 is the second wireless receiver in the system. Together, TRM2 and RCV2 wirelessly transmit and receive the serialized data generated by the output shift register. They both operate at 914 MHz and transmit data at 115.2 Kbps.

9. **Teradyne J750 – receive data**. The Teradyne J750 must be configured to receive the outputs from the DUT. In order to receive outputs from the DUT, an input on the J750 must be mapped to a channel and the expected waveform to be received must be programmed.

10. **Viewing the output data**. The data will be sent in a serial stream such that there is a leading 1, and then the two outputs from the DUT will follow immediately after the leading 1. After the two outputs, a long string of 0's will be transmitted to create a quiet period before the next leading 1 is sent. In this way, it will be obvious when a data transmission begins, and will facilitate reading the values of the DUT output by inspection.

Resources and Schedule

A summary of the number of hours that will be spent by each group member is shown in Table 1 below.

Table 1: Summary of team member hours

	Nathan Gibbs	Dan Holmes	Adnan Kapadia	Kyle Peters	Total
Hours	258	255	256	258	1027

A summary of the total financial commitment that the project requires is shown in Table 2 below.

Table 2: Financial summary of project

Hardware	Labor at $11.00/hr	Total
$83.67	$11297.00	$11380.67

The Gantt chart of the deliverables for the project is shown in Figure 4 below. A more detailed Gantt chart is included with the full report.

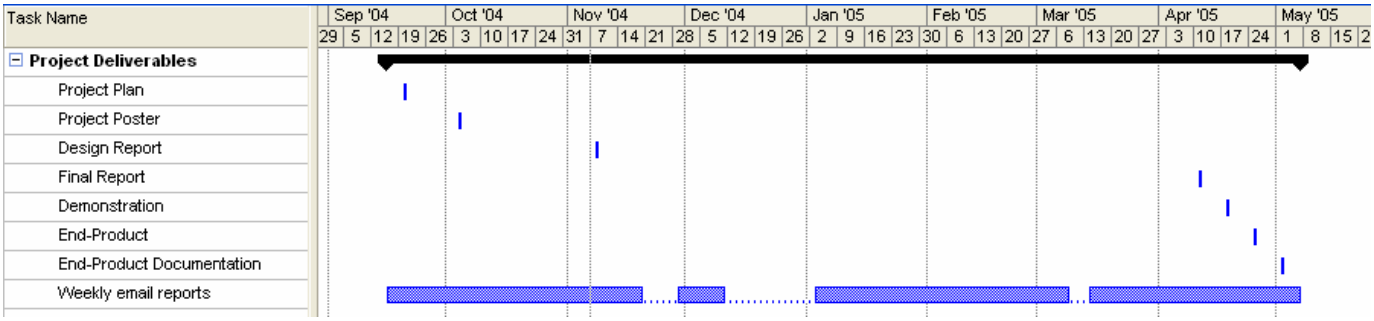

Figure 4: Project Deliverables

Conclusion

The need for reliable wireless testing is growing. This project will investigate the feasibility of a system by which the Teradyne J750 can remotely test a device through a wireless send/receive network. If the system is successful, the project will prove that the J750 can perform wireless tests and will pave the way for more projects using wireless tests. If the system is unsuccessful, the project will provide good documentation for future users that wish to pursue wireless testing.

Today, hundreds of companies are producing wireless LAN cards and routers. But to make sure these products perform as needed, high speed testing of the RF components is necessary. Iowa State University has an excellent tester, the Teradyne J750; however the J750 cannot currently test devices wirelessly.

The purpose of this project is to investigate if it is possible for the Teradyne J750 to remotely test a DUT. In order to investigate this, the team will develop a wireless send/receive network between the Teradyne and the DUT. The team will attempt to use this send/receive network to test the DUT. If it is possible, the team will create a working demonstration, and write a manual for future users to set up wireless tests. If it is not possible, the team will document its findings and pass them along to Teradyne.

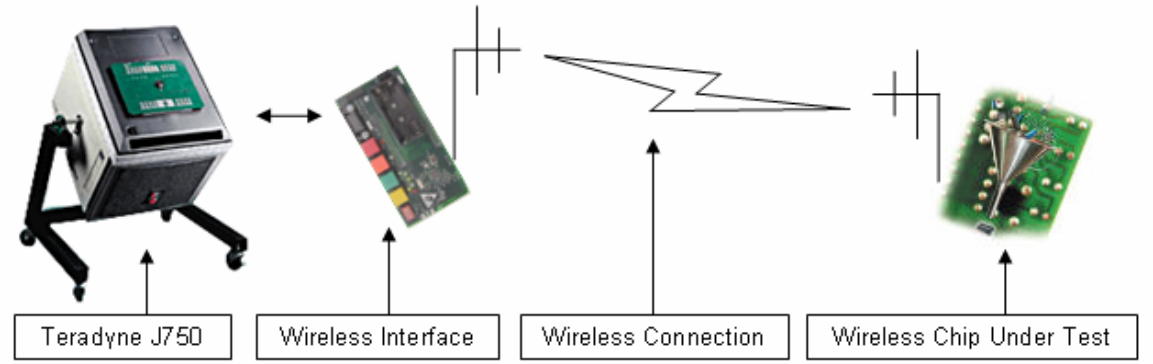

Figure 5: Block diagram of proposed solution

1.2 Acknowledgements

The team would like to take the opportunity to thank Dr. Robert Weber for his commitment to advise the team through the course of the project. The team would also like to thank Bernard Lwakabamba for his help on the TI wireless LAN chips. Additional acknowledgement goes to the Carver High Speed Systems Lab for allowing the team to use the PCB milling machine.

1.3 Problem Statement and Solution

This section shall outline the general problem as well as an overview of the proposed solution.

1.3.1 Problem Statement

Testing is a major part of the development process for almost any product. Products must be tested before they can be marketed to ensure that they work as they should. Educational institutions need to be highly involved in research and testing. Knowing this, many companies will donate testing equipment to help with their research. This is the case with Teradyne's donation of their Teradyne Integra J750 tester.

Iowa State University's Department of Electrical and Computer Engineering is interested in using two transmitter chips paired with two receiver chips to give the Teradyne Integra J750 Test System a wireless send/receive network interfaced with a DUT. Using the S/R network, the Teradyne J750 would be able to test the DUT. However, there is currently no way to interface the Teradyne J750 to the S/R network. Also, if an interface is made, it is unknown if the Teradyne J750 can receive a reply from a transmitter on the DUT side of the network. This is because there is a delay between when a signal is sent through the network to the DUT and when the DUT side of the network replies. The J750 is not usually used under such unknown delay conditions, so this project will assess the feasibility of using the J750 under such conditions, and try to develop a solution that will allow the J750 to receive a reply from the wireless chip after some unknown delay.

1.3.2 Problem Solution

A device interface board (DIB) will be used to connect the transmitter chip (TRM1) and the receiver chip (RCV2) to the Teradyne J750. Figure 6 shows a block diagram of the proposed setup. Test code will be developed for the Teradyne to interface with the S/R network. An FPGA will be used to interface the receiver chip (RCV1) with the DUT. The same FPGA will be used to interface the results from the DUT with the transmitter chip (TRM2). The team will develop solutions to test and make operational the I/O on TRM1 and the device under test. When all components are known to work, the team will develop a solution (or solutions if the first fails) to make the J750 test the DUT. It is unknown if a solution exists, so the team will need to try multiple solutions to solve the delay problem.

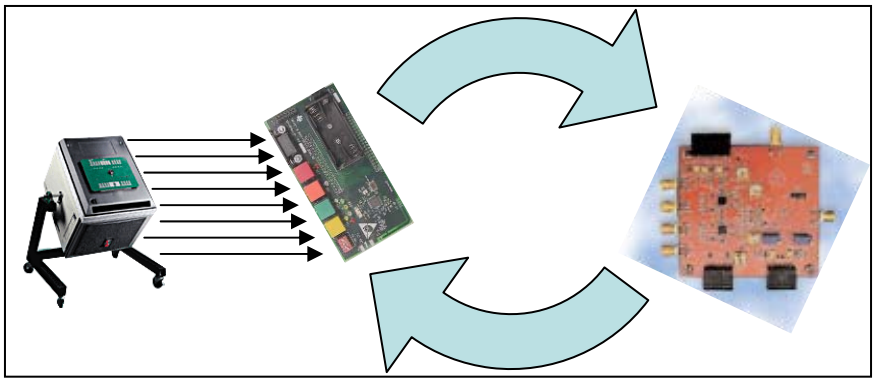

Figure 6: Overview of problem solution

1.4 Operating Environment

The operating environment for the finished setup is indoors from 27°C to 33°C. It should not be subject to ESD or mechanical shock. This is because only the client will use the J750 and the wireless send/receive network indoors in an air conditioned room. Because all components are expensive and all users are expected to treat the setup with care, the chance of mechanical shock is limited. Also, the J750 is sensitive to temperature and can only be used from 27°C to 33°C, so the entire project will only be used in that temperature range. Lastly, because the J750 is so sensitive, users are required to wear an ESD band while using it, so the project should be safe from ESD.

The code for the interface between the J750 and S/R network will be developed using the program IG-XL, the J750 interface development program. The PC on which IG-XL currently runs is a Windows-based PC.

1.5 Intended User and Intended Use

This section defines the intended users and uses of the project.

1.5.1 Intended User

The intended user is any member of the ECpE department that needs to test the RF capabilities of a wireless device. The size and sex of the person doesn't have any bearing on their ability to test, however they must posses a basic knowledge of RF communication and understand how to run a test on the J750. Specifically, they must be able to make the frequencies of the FPGA and the data rate of the S/R network the same, and follow the reference manual created for this project to allow the J750 to remotely test the operation of a DUT.

1.5.2 Intended Use

The intended use of the project is to allow the J750 to send a single signal wirelessly through TRM1 to a DUT. The DUT should receive the signal, process it, and send a signal back (the signal sent to the DUT will instruct the DUT to perform a diagnostic test and send back a reply) and the J750 will receive the reply through the S/R network.

The setup is only intended to test a single DUT, it is not meant to monitor network traffic or multiple devices. Also, it is not meant to test all of the components of the DUT such

as delay or signal strength, just the desired digital operation of the device. Sending the DUT a signal to perform a diagnostic test simply creates output for it to send to the J750.

1.6 Assumptions and Limitations

This section defines the assumptions and limitations for the end-product. Assumptions and limitations will be added as decisions are made in regards to the project.

1.6.1 Assumptions

This section will provide details of the user and system assumptions:

1.6.1.1 User Assumptions

This section will discuss the assumptions the team made for the user.

- User knows English – The user-documentation will be written in English.
- User is well educated in electrical and/or computer engineering. Specifically user understands need to have data rate of the S/R network greater than the processing speed of the FPGA and DUT.
- User is aware of electrical hazards (short circuits, overloading, etc.).
- User is experienced with circuit testing using the Teradyne J750.
- User has access to Teradyne lab in Coover Hall.
- User will observe ESD requirements around Teradyne J750.
- User will have knowledge of FPGA usage, specifically the Verilog or VHDL programming languages.
- User understands how a shift register operates.

1.6.1.2 System Assumptions

This section will discuss the assumptions the team made for the system.

- Teradyne can interface with the S/R network with an existing daughterboard or a custom designed interface board.
- The data rate of S/R network and the DUT operate at one frequency.
- Setup will only test one DUT at a time
- Teradyne J750 can receive a reply from wireless device after unknown delay period.
- FPGA will operate on an infinite loop.
- PLL will drive the clock input for the FPGA.

1.6.2 Limitations

This section will provide details of the limitations identified with the project:

- The Teradyne system is operating within ±3°C of its calibrated temperature. (30°C for the current system)
- The Teradyne system can only test digital I/O. Therefore, all wireless chips must have digital I/O.
- Unable to use the setup if there are nearby wireless signals at similar frequencies.

- The Teradyne J750 is stationary, so operating environment shouldn't change.
- IG-XL software has the ability generate test codes for wireless LAN chips.
- Range of the transmitter and receiver pairs are great enough to interface with wireless device under test.

1.7 Expected End-Product and Other Deliverables

This section will provide the details of the expected end-product and other deliverables. By the end of spring 2005 the project will result in:

- An electrical and wireless interface between the Teradyne J750 and the S/R network.
- A strong communication link between the two transmitter/receiver pairs, including the interface with the DUT between the two pairs. This means that S/R network can send and receive signals around the loop (from the Teradyne to the DUT and back to the Teradyne). It is unknown if the J750 can process the received signal after an unknown delay, which is a problem to be studied.

If the J750 can process an input from the output of the DUT:

- A demonstration to test the digital components on a D flip-flop (DUT) using the Teradyne J750.
- A reference manual on how to remotely test a device using the Teradyne J750.

If the J750 cannot receive a reply from the DUT:

- A document explaining the failure of the project.
- A full report to be given to Teradyne regarding the project.

2. Approach and Product Design Results

The approach and product design results will provide a detailed description of the end-product design and the approach used to successfully attain the design objectives.

2.1 Approach Used

This section will provide the details of the design objectives, functional requirements, design constraints, technical approach considerations and results, testing approach considerations, and recommendations regarding project continuation or modifications.

2.1.1 Design Objectives

The following objectives describe the functional requirements to meet the client's objectives:

- Develop an interface between the Teradyne J750 and RFM transmitter (TRM1).

- The output (test data) from the Teradyne J750 will be serialized in order to be transmitted on a 900MHz frequency channel.

- Develop an interface between the RFM receiver (RCV1), transmitter (TRM2) and DUT.
    - The data received by the transmitter on the DUT side will be de-serialized (parallel output) and presented to the input pins of the DUT.

    - The output data from the DUT will be serialized and transmitted back to the Teradyne J750.

- User manual for future users - Develop a user friendly manual to operate the Teradyne J750 to test DUTs wirelessly.

2.1.2 Functional Requirements

The following section describes the functional requirements of the end product in detail:

- Successful data transmission from Teradyne J750 to transmitter (TRM1). The interface should not lose any data while serializing the output of the Teradyne J750 to present to the input of the transmitter (TRM1).

- Strong communication link between transmitters and receivers. The wireless communication link should not increase the SNR due to other electrical appliances present in the test lab.

- Half-duplex system - Only one transmitter (TRM1) and one receiver (RCV1) at different frequencies make this system half duplex.

- No interference in communicating between TRM1/RCV1 and TRM2/RCV2. In order to avoid cross talk between TRM1/RCV1 and TRM2/RCV2 the communication channel will be at separate frequencies (914MHz & 916MHz).

- Successful data transmission from receiver (RCV1) to DUT. The interface should not lose any data and have low bit error rate while de-serializing the output from the receiver when presenting to the DUT.

- Successful data transmission from DUT to transmitter (TRM2). The interface should not lose any data while serializing the output from the DUT to present to the transmitter.

2.1.3 Design constraints

The following will describe the constraints on the design for a completely functional end product:

- Limited to one software type on the Teradyne J750. Since the Teradyne J750 uses IG-XL, which is essentially a Visual Basic and Excel platform. The team is limited to drawing user interfaces only in Basic.

- Limited to using only one frequency for communication. Due to lack of hardware and to keep the product easy to use the team will use one frequency for data transmission.

- Required to slow down the data rate on the Teradyne J750. Due to the lack of speed on the PLL, RFM receivers/transmitters, and shift registers the team will be slowing down the date rate from the Teradyne J750 to avoid loss of data.

- The distance between the receivers and transmitters is limited to less than 5 feet. Due to limited space (floor area) in the Teradyne lab the team will be testing the RF transmission strength to less than 5 feet range.

- The operating conditions are limited to 30°C ± 3°C. As per the specification of the operating temperature, the lab temperature will be held between 27°C and 33°C

- The budget for the project is limited to $150.00. The team would like to thank Dr. Weber for the receivers and transmitters but all other expenses were limited to $150.00

- The Teradyne lab is only accessible by selected faculty members and students. Due to department rules and regulations the team will only be able to provide

this product to selected faculty members and students who have access to the Teradyne lab in Coover Hall.

- Limited to using one FPGA. The team would like to use 4 FPGA's to serialize and de-serialize the data for transmission but due to lack of funding the team limited the design to have only one FPGA on the DUT side.

- One modulation scheme. To avoid complexity the team chose to use either the FSK or ASK modulation schemes. Also this option helps design the PLL to lock on to the correct phase of the incoming data.

- The user is aware of the Teradyne J750 and has used it prior to using this product. Also the user will observe ESD precautions around the Teradyne J750 as shown in Figure 7 below.

Figure 7: ESD wrist band

2.1.4 Technical Approach Considerations and Results

This section presents several technology alternatives analyzed during the design of the product and the technology selected for the final design.

2.1.4.1 Device Under Test

The team had to decide the device under test to be used in testing for complete functionality of the end product. There were two main considerations for the device under test:

- **Random Access Memory.** The team considered using a DRAM 256Mbit part for the device under test. Being a pure digital component, DRAM can easily be tested by checking for the stored bits and matching them to the input data. The second advantage is that one of the team members has experience in operating DRAM and testing it

for full functionality. For this project using DRAM as the device under test had several disadvantages. Firstly, it is difficult to test all 256M bits at once. Secondly, it is difficult to obtain only one packaged part as most of the DRAM sold today are sold in modules (on PCB's). Thirdly, the team would also need to develop or purchase a daughterboard to match the input and output pins of the DRAM module to the Teradyne J750.

- **Positive edge triggered D flip-flop.** The team considered using a positive edge triggered D flip-flop for the device under test. It has four inputs and two outputs making it easy to test. A D flip-flop operates on simple logic avoiding further debugging steps caused by the DUT. Also the team has tested a D flip-flop using the Teradyne J750 making it simpler to debug. For this project, a D flip-flop had one disadvantage. It would reduce the usability of the product as many industries do not use the Teradyne J750 to test a D flip-flop.

Selected device under test: *Positive-edge triggered D flip-flop*
The team decided to use the positive edge triggered D flip-flop as the device under test. The simplicity of the inputs and outputs is advantageous to the design of this product. Also since most of the members understand the logic behind a D flip-flop it makes it easier for the team to concentrate on the product design. Although it may be perceived to be an inferior DUT, it can be scalable to complex digital systems.

2.1.4.2 Parallel to serial data converter

The parallel to serial data converter is required because the Teradyne J750 outputs the data in a parallel format and in order to transmit the signal on a wireless channel the team needs to convert it into a serial data stream. As the team chose a D flip-flop to test there are 4 main inputs that need to be sent to the parallel to serial converter as shown in Figure 8.

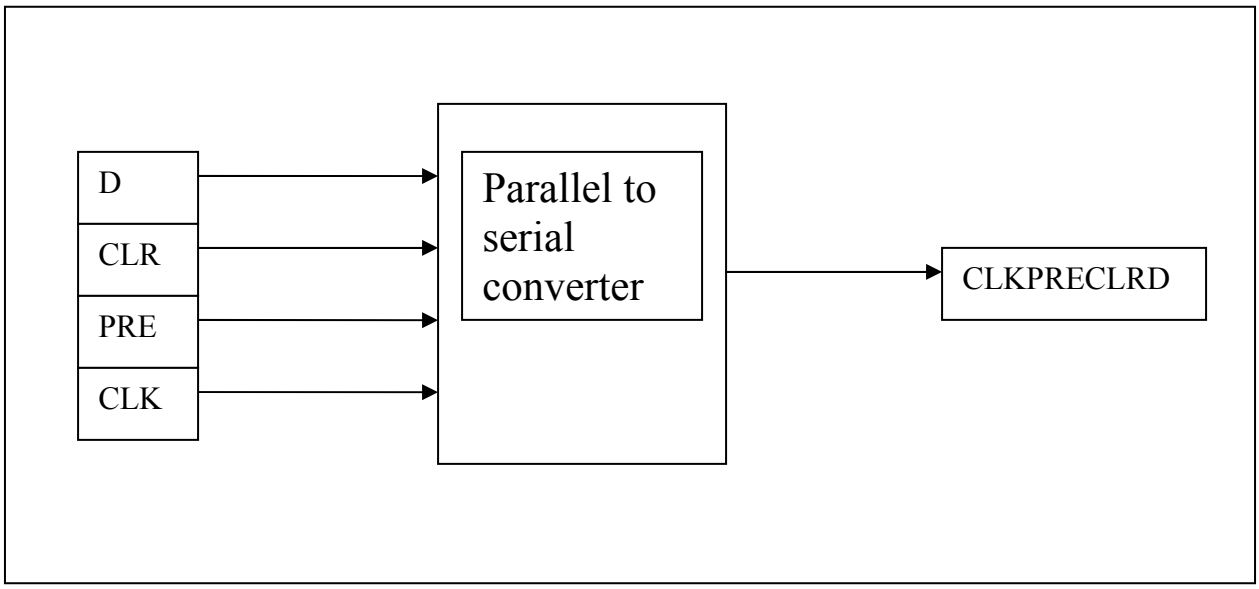

Figure 8: Block diagram of parallel to serial data converter

- **Shift Register.** The team considered to use a 16-bit shift register to convert the parallel data into a serial data stream. The main disadvantage of this consideration is the data rate limitation. The Teradyne J750 outputs data at 100Mbps and most of the shift registers in the industry operate at 25Kbps. The key advantage was a part readily available that would convert parallel data into serial data. Also the cost of a shift register was nominal (~8cents), which would help keep the team on track with the budget assigned.

- **FPGA – Field Programmable Gate Array.** The team considered to use a standard FPGA and develop code to convert the parallel data into serial data. The main disadvantage was the cost of purchasing a FPGA, as it approximately costs $250 a piece. The advantage was that the team was familiar with FPGA's as all the team members have used it in previous courses.

Selected parallel to serial data converter: *Shift Register*

The team decided to use a standard 16 bit shift register to convert the parallel data from the Teradyne J750 into a serial data stream to transmit wirelessly. The main reason the team chose the shift register is the unavailability of funds to purchase additional FPGA's. Also the shift register is smaller and easier to mount on the Teradyne J750. The team did realize that the data rate would be slower but the trade off had to be made due to lack of funds.

2.1.4.3 Wireless communication system

The team had to research all possible wireless communication methods to match the requirements of the end product. The two main requirements of the communication methods were:

- Two different frequency channels for transmitting the input data from the output data.
- Fastest data rate to match the Teradyne J750.

Appendix C shows the research conducted by the team to gain insight on products available in the market. The three main objectives were frequency, data rate and cost.

- **Transceivers.** The team considered using two transceivers for the two-way communication of data. The first being the data coming in from the Teradyne J750 into the DUT and the second being the response of the DUT back to the Teradyne J750. The two main disadvantages of using transceivers were the data would be transmitted at one frequency with different modulation schemes and the system would be full duplex. The main advantage for this project would be to cut down the overall cost of the project.

- **Individual receivers and transmitters.** The team considered using individual receivers and transmitters. There was one main criterion to evaluate, frequency. The two options are listed below:
  - 2.4GHz receiver and transmitter. The team considered using a 2.4GHz receiver and transmitter in order to transmit the data at a quicker rate. The one disadvantage was that many appliances, for example microwaves, operate at this frequency which could affect the SNR.

  - 900MHz receiver and transmitter. The team considered using a 900 MHz receiver and transmitter as it is easier to use and it has simple modulation schemes (FSK and ASK). The main disadvantage with this option was the slow data rate.

Selected wireless communication system: *900MHz receiver and transmitter*

The team decided to use the 900MHz receiver/transmitter pair from RF Monolithics as the product could have two separate frequency channels (914MHz & 916MHz) and it uses simple modulation schemes. The team decided to go with a slower data rate as it was apparent that the team would have to slow down the Teradyne J750 in order to avoid loss of data while converting the system I/ O from parallel to serial using the shift register.

2.4.1.4 Serial to parallel data converter

The end-product is required to have a serial to parallel converter as the DUT chosen requires all the inputs at one instant in time to produce a meaningful output.

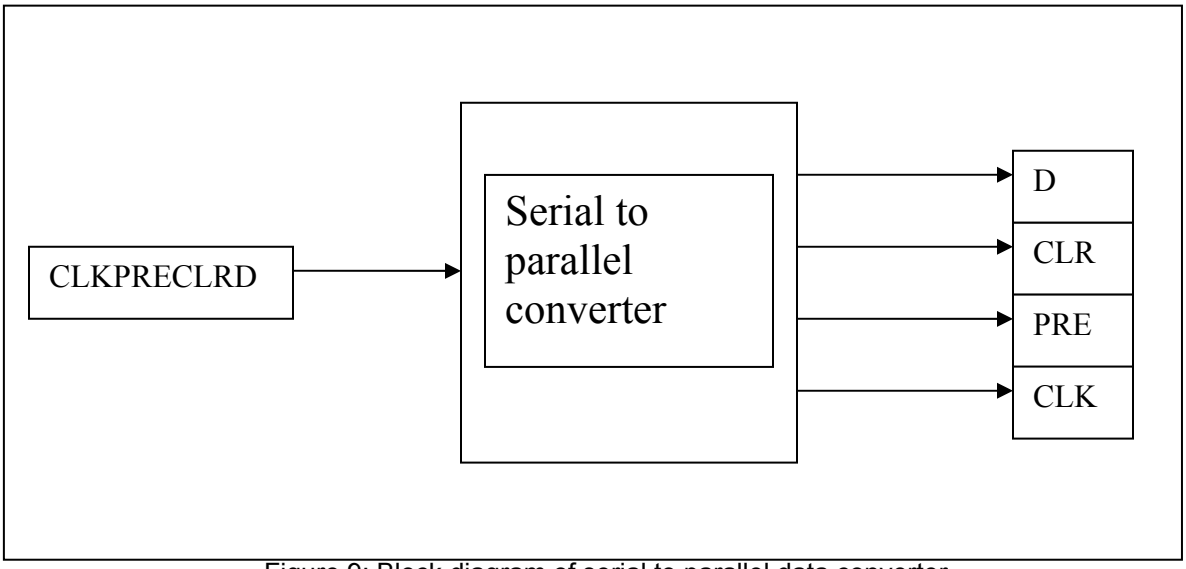

Figure 9: Block diagram of serial to parallel data converter

- **FPGA – Field Programmable Gate Array.** The team considered an FPGA for the serial to parallel data converter. It is easy to code and develop a serial to parallel shift register in an FPGA. It also has its own memory module to store all the converted data and present it directly to the D flip-flop. Once again, the main disadvantage of an FPGA was the cost factor.

- **Shift register.** The team considered a simple 16-bit serial to parallel data converter. As these registers are easy to use and are capable of performing the required operation without additional coding. The main disadvantage here being that the clock signal would have to be within specific limits to avoid data loss.

Selected Serial to parallel converter: *FPGA*

The team chose to use the FPGA as the computer engineers on the team were comfortable with coding a shift register. Also the FPGA has a built-in memory module to store the converted data, which removes the possibility of using separate memory devices to store data. This option would also reduce the cost of the project, as the FPGA to be used has been donated by the ECpE department. Overall the FPGA would perform a dual purpose on the DUT side: firstly to convert data from serial to parallel and secondly to convert its inputs from the DUT from parallel to serial.

2.1.4.5 Language for coding the FPGA

The team had to decide the programming language to be used for the FPGA being used:

- **Verilog.** Verilog is a hardware description language used to describe gate level representations of CMOS logic. It is easy to learn and use. The flexibility of this language enables the team to write code quickly and accurately.

- **VHDL.** VHDL offers precision at the cost of simplicity. It is an alternate hardware description language used by the industry for describing the gate level representations as text.

Selected Language for coding the FPGA: *Verilog*
The team decided to use Verilog as it is a language the entire team is familiar with and requires less time to code.

2.1.4.6 Clock recovery circuit

The project requires a clock recovery circuit to generate a synchronized clock that feeds in to the FPGA. The FPGA will then use the clock signal to sample the data correctly on the DUT side to convert it into a parallel output.

- **Phase Locked Loops.** The team considered using phase locked loops to recover the clock signal at which the data was sent wirelessly. Appendix B has a more detailed description on how PLL's work. The main advantage of a PLL was that the team would not have to test the frequency at which the data was coming in, as the PLL would automatically lock on to the right phase and generate the clock. The disadvantage of this option was that none of the team members were aware of this circuit and its operation.

- **Crystal oscillator.** The team considered implementing a crystal oscillator that generates a clock signal at a tuned frequency. This option could be used if the user knows the data rate at which the data was being sent. The advantage being the team would not have to worry about debugging as all it needs is the correct tuning. The disadvantage of the oscillator was that every time the data rate changed the user would have to physically tune the crystal oscillator to the correct frequency.

Selected clock recovery circuit: *Phase Locked Loop*
The team decided to use a Phase Locked Loop to recover the clock signal. This was the best solution as it could be used for any data rate and is self tuned to the right phase. This circuit uses its own "intelligence" to recover the clock signal instead of being physically tuned like the crystal oscillator.

2.1.5 Testing approach considerations

Each subsection of the final product will be tested thoroughly and will be evaluated according to the design requirements. These are the subsections that will be tested individually:

- Shift register
- Transmitters (914MHz and 916MHz)
- Receivers (914MHz and 916MHz)
- FPGA
- Phase-locked loop

Here is a sample form that will be used to test/retest each of the above mentioned parts:

Name:_____
Date & Time:_____
Test description: _____
_____

1.	Is the part enabled/powered up	Y	N
2.	Is the input data exactly what is being generated	Y	N
3.	Is the output as expected theoretically	Y	N
4.	Are there multiple harmonics of the signal (receiver and transmitter only)	Y	N
5.	Is the clock synchronized with the input clock (PLL only)	Y	N

Measurements

Frequency of the transmitted signal: _____
Data rate of the transmitted signal: _____
Frequency of the shift/enable signal: _____
(shift register only)
Frequency of the phase-locked loop clock signal: _____

Comments:
_____
_____
_____
_____
_____

After each part is tested the entire setup will be tested for latency and timing issues to ensure full data transfer without any distortion. The team will also select a few faculty members to use the setup for their particular tests. This will spare the team redesign or improve small glitches present in the setup.

The tests will all be conducted in the Teradyne lab in Coover Hall, and once each subsection is tested by team members, faculty will be invited to test their wireless devices in the system.

2.1.6 Recommendations regarding project continuation and modifications

The team recommends that the project should continue as envisioned. This section details the recommendations for future work on the project. The team's recommendations maintain the original goal of the project.

The team will develop a completely functional setup in which a D flip-flop can be tested wirelessly. This will empower the user to test a DUT from any location he/she wishes. In the future the user could also test RF transceivers for RF signal strength.

The following recommendations would increase the usability of this product for the future:

- Test various DUT's for more flexible use
- Increase distance between DUT and Teradyne J750
- Develop proprietary modulation schemes for data transmission
- Implement quicker and smaller data converters

2.2. Detailed Design

The detailed design section of this report features a thorough description of the design of the final wireless S/R network.

2.2.1 Overview of the system design

As previously stated, the purpose of the system is to wirelessly test a device using the Teradyne J750. In order to do so, the system takes input signals from the Teradyne J750, sends them across a wireless connection performs the test on the DUT and sends the output of the DUT back across a wireless connection to the Teradyne J750. A block diagram of a system overview is shown in Figure 10 on the next page. Each of the major subsystems are numbered in the figure. The major subsystems of the design are listed below and will be discussed in greater detail in the following sections:

- Teradyne J750 - inputs
- Input shift register
- TRM1, wireless connection and RCV1 – input signals
- PLL
- FPGA
- DUT
- Output shift register
- TRM2, wireless connection and RCV2 – output signals
- Teradyne J750 – receive data

- Viewing the output data

For all designs, Dr. Weber has donated the use of the Carver High Speed Systems Laboratory, so all PCBs that will need to be created to implement the design will be fabricated in the Carver laboratory.

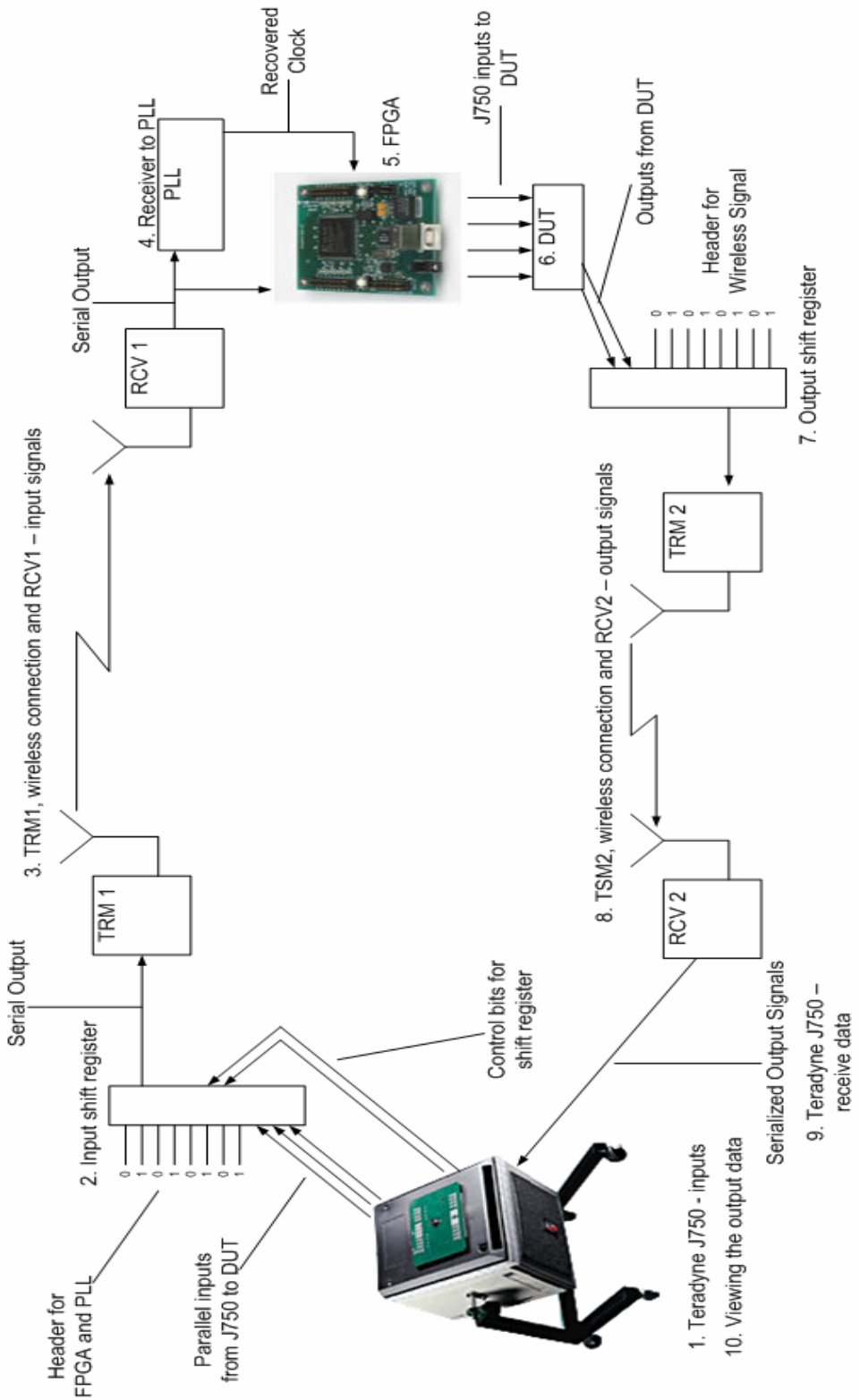

Figure 10: Block diagram of end product solution

2.2.2 Teradyne J750 – inputs

The purpose of the Teradyne J750 is to generate inputs to stimulate the DUT, and generate a clock and load signal to control the input shift register. The Teradyne J750 is seen below in Figure 11:

Figure 11: Teradyne J750

In order to create an input signal, one must follow the flowchart seen in Figure 12 below.

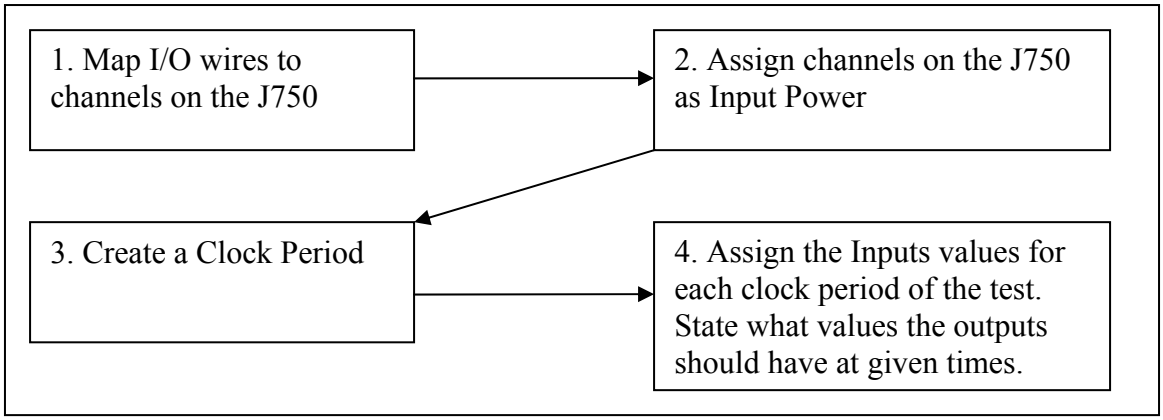

Figure 12: Flowchart to create an input signal

The team has already used the Teradyne J750 reference manual to understand the I/O of the Teradyne J750, and has used the manual to create a test for a D flip-flop. The team can follow the same procedure to produce the input signals to the DUT in this system as well.

The clock and load signals, which will control the input shift register, will also be created using the same methods used to create the input signals to the DUT. The timing of the signals will be chosen to allow the shift register to load the parallel inputs to the DUT and shift them out to TRM1.

2.2.3 Input shift register

The purpose of this portion of the system is to take the inputs from the Teradyne J750 serialize them, and attach a header so that they can be sent to TRM1 (the transmitter only accepts serial inputs). A block diagram of the shift register is shown in Figure 13:

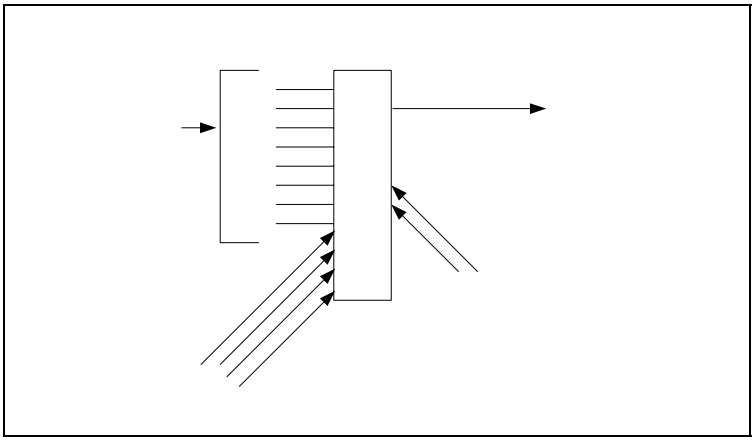

Figure 13: Block diagram of shift register

The shift register has 16 parallel inputs, and two control inputs. Four of the 16 parallel inputs will be the inputs to the DUT generated by the J750. The other 12 inputs will be tied to 3 volts and 0 volts in an alternating pattern – this is done so that when the parallel outputs are shifted out of the register, the digital pattern of 101010101010 (3 volts, 0 volts, 3 volts 0 volts etc. – the digital values of these voltages are 1 and 0) will serve as a header for the packet of data.

The header is present so that the PLL can recover the clock signal and feed the clock signal to the FPGA. The FPGA will then use the clock signal to read the data, and can use the header to identify the 12-bits preceding the 4-bits of input data from the Teradyne J750.

Also, the two control inputs to the shift register generated from the Teradyne J750 are the clock pulse and the mode select bit. The operation of the shift register is such that when the mode select bit has 3 volts input and the clock goes from 3 to 0 volts, all of the inputs on the parallel inputs will be loaded into the shift register. Then when the Load/Send bit has a 0 volt input and the clock goes from 3 to 0 volts, all of the parallel inputs that have been loaded will be shifted out in a serial stream of data. A summary of the operation of the shift register is shown in Table 3 below:

Head
FPGA a

Table 3: Summary of operation of shift register

Mode Select	Clock pulse	Function performed
3 V	3 V to 0 V	Load parallel inputs
0 V	3 V to 0 V	Shift parallel inputs out in serial data stream.

The Teradyne J750 will generate clock and load/send control inputs to make the shift register shift in parallel inputs and shift out serial data at 115.2 Kbps as that is the highest data rate the TRM1 can support. This setup is ideal because it does not require any extra processors on the transmit side of the wireless system – the J750 provides all the control and input bits that are required to create a serial stream of data, with a header at 115.2 Kbps.

The team has chosen to use the Fairchild Semiconductor 74F676PC shift register. The part is a 16-bit parallel to serial shift register and that can operate up to 25 MHz. It is simple to use, cheap and is fast enough for the application. Its data sheet is attached in Appendix D. The circuit diagram the team will implement is shown in Figure 14.

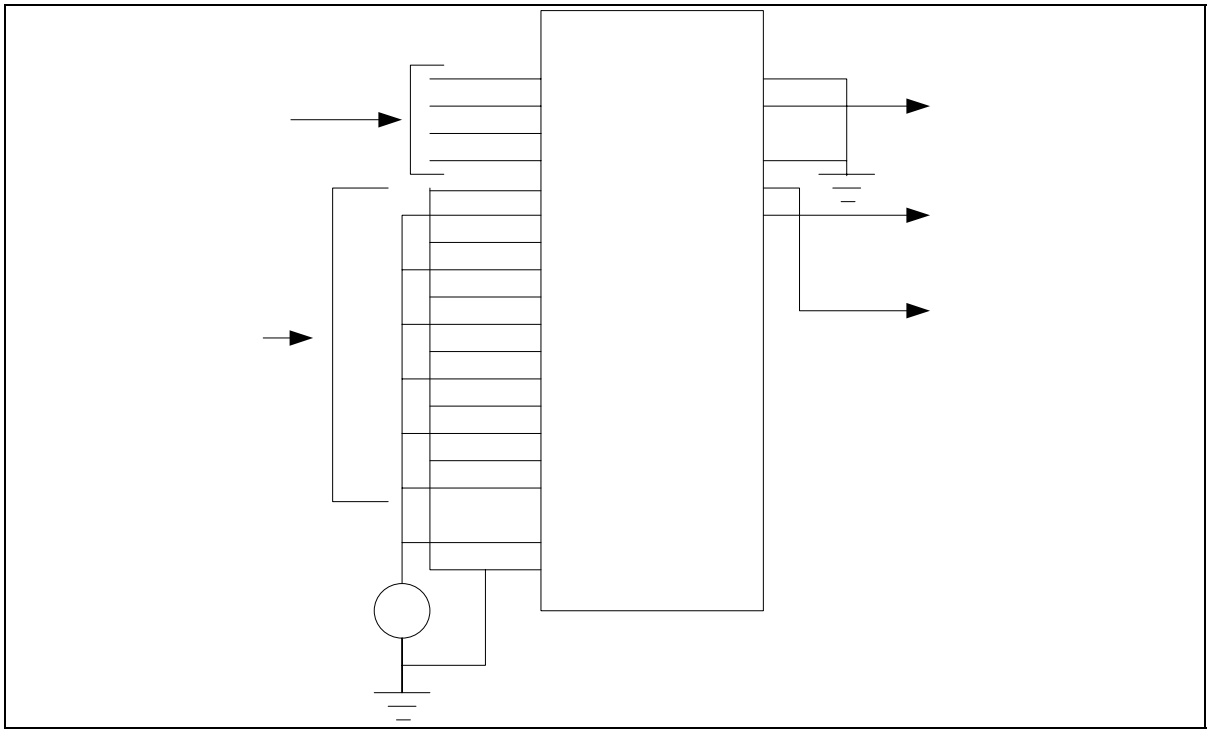

Figure 14: Circuit schematic of shift register

2.2.4 TRM1, wireless connection and RCV1

The purpose of TRM1 and RCV1 is to wirelessly transmit and receive the serialized inputs from the Teradyne J750. The TRM1 will take the serialized output (with header preceding the data) from the shift register, and use ASK modulation to send the wireless signal to the RCV1 module. The RCV1 module will receive the signal, demodulate it, and present the signal transmitted in a serial stream. A block diagram of the setup is shown in Figure 15 on the next page.

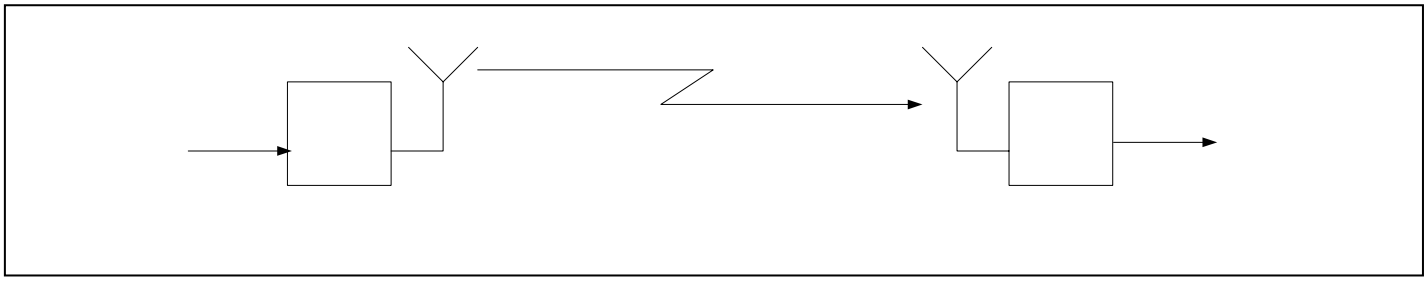

Figure 15: Block diagram of wireless setup TRM1 to RCV1

The group has chosen a transmitter and receiver from RF Monolithics to implement this subsystem. The parts chosen are the TX 6000 (transmitter – TRM1) and RX 6000 (receiver – RCV1). Their data sheets are attached in Appendix D. They communicate at 916.5 MHz, and Dr. Weber has donated the antennas for both the TX and RX 6000 components. The TX 6000 can transmit data up to 115.2 Kbps and the RX 6000 can receive data at rates up to 115.2 Kbps. This is why the shift register will receive a clock signal from the Teradyne J750 to shift out data at 115.2 Kbps – the TX 6000 can only send data at 115.2 Kbps.

In order to make the TX 6000 operate in ASK modulation, the circuit schematic seen in Figure 16 will be created.

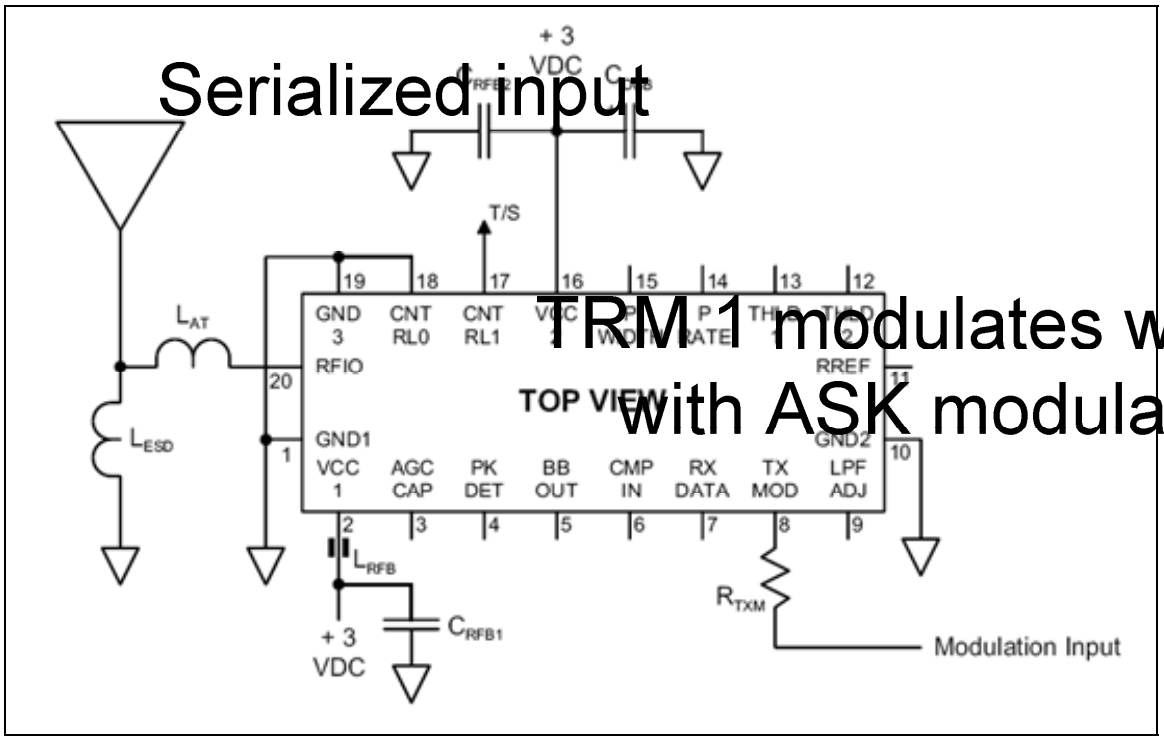

Figure 16: Circuit schematic for TX 6000

The parts that will be used to create the circuit (aside from the TX 6000) are listed in Table 4 on the next page.

Table 4: Part list for TX 6000

Part	Value	Specification
TXMOD Resistor RTXM	4.7 K	±5%
DC Bypass Capacitor CDCB	4.7 µF	±5%, tantalum
RF Bypass Capacitor 1 CRFB1	27 pF	±5%
RF Bypass Capacitor 2 CRFB2	100 pF	±5%
Series Tuning Inductor LAT	10 nH	±5%
Shunt Tuning/ESD Inductor LESD	100 nH	±5%

Similarly, the circuit schematic to make the RX 6000 receive data modulated using ASK is shown in Figure 17.

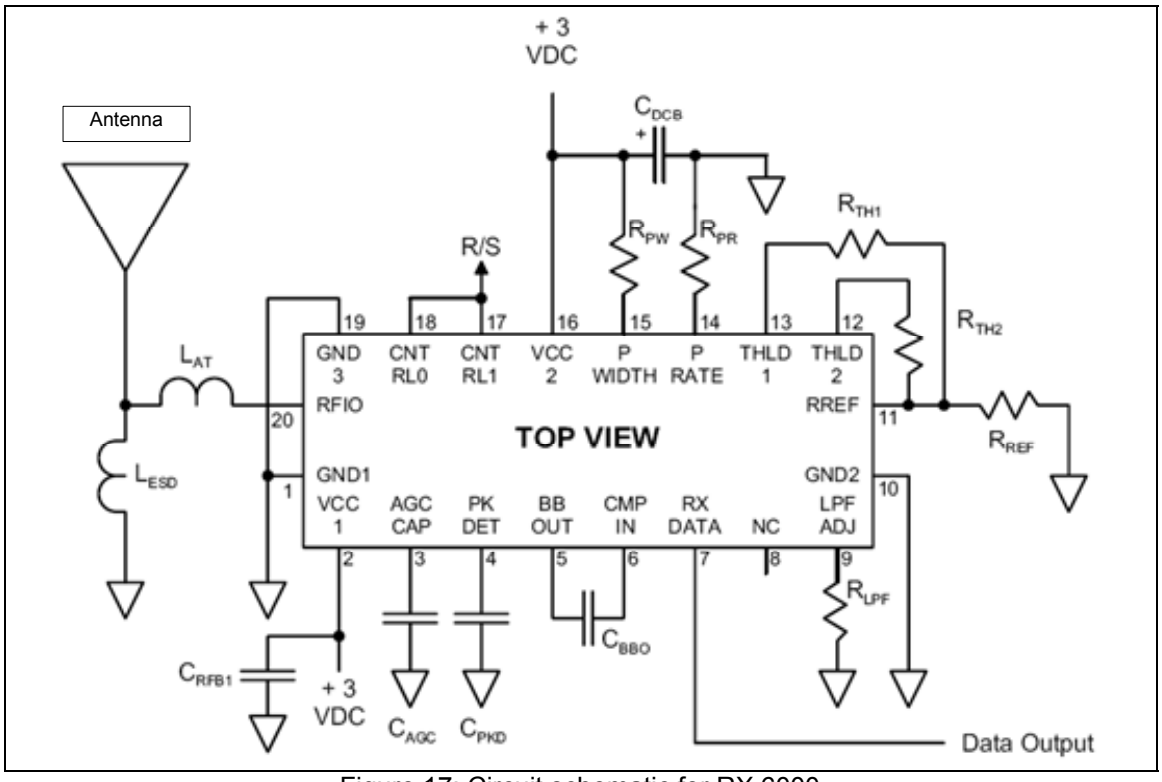

Figure 17: Circuit schematic for RX 6000

The parts that will be used to implement the circuit (aside from the RX 6000) are listed in Table 5 on the next page.

Table 5: Part list for RX 6000

Part	Value	Specification
Capacitor CAGC	2200 pF	±10% ceramic
Capacitor CPKD	0.001 µF	±10% ceramic
Capacitor CBBO	0.0027 µF	±10% ceramic
Resistor RBBO	0 K	±5%
Resistor RLPF	15 K	±5%
Resistor RREF	100 K	±1%
Resistor RTH2	100 K	±1%
Resistor RTH1	10 K	±1%
Resistor RPR	160 K	±5%
Resistor RPW	1000 K	±5%
DC Bypass Capacitor CDCB	4.7 µF	±5% tantalum
RF Bypass Capacitor 1 CRFB1	27 pF	±5%
Antenna Tuning Inductor LAT	10 nH	±5%
Shunt Tuning/ESD Inductor LESD	100 nH	±5%

The schematics and parts were taken from the TX 6000 and RX 6000 datasheets as recommended circuits and component values to bias the parts for operation in ASK mode.

2.2.5 PLL

The purpose of the PLL is to recover the clock signal of the data sent wirelessly. The clock signal will then be fed into the FPGA so that the FPGA will have the correct clock reference to read the data. For more information on how a PLL works see Appendix B.

The demodulated, serial data from the RX 6000 (RCV 1) will be fed into the PLL. The PLL tries to recognize the frequency of change between a logic 1 (3 volts) and logic 0 (0 volts). From the changes between 1 and 0, it generates a clock output at the same frequency as the input signal. So, the header of 101010101010 is fed into the PLL and the PLL generates a clock signal at the same frequency the data is transmitted. The FPGA can then use this clock signal to operate and know at what frequency to read in the transmitted data. The block diagram for this portion of the system is shown in Figure 18.

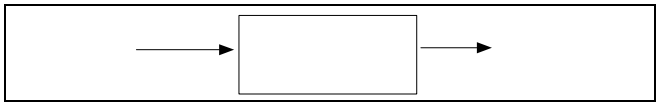

Figure 18: Block diagram of a PLL

The PLL chosen is the CD74HC(T)7046, manufactured by Texas Instruments. Its data sheet is attached in Appendix D. The circuit schematic that will be used to implement the system is shown in Figure 19 on the next page.

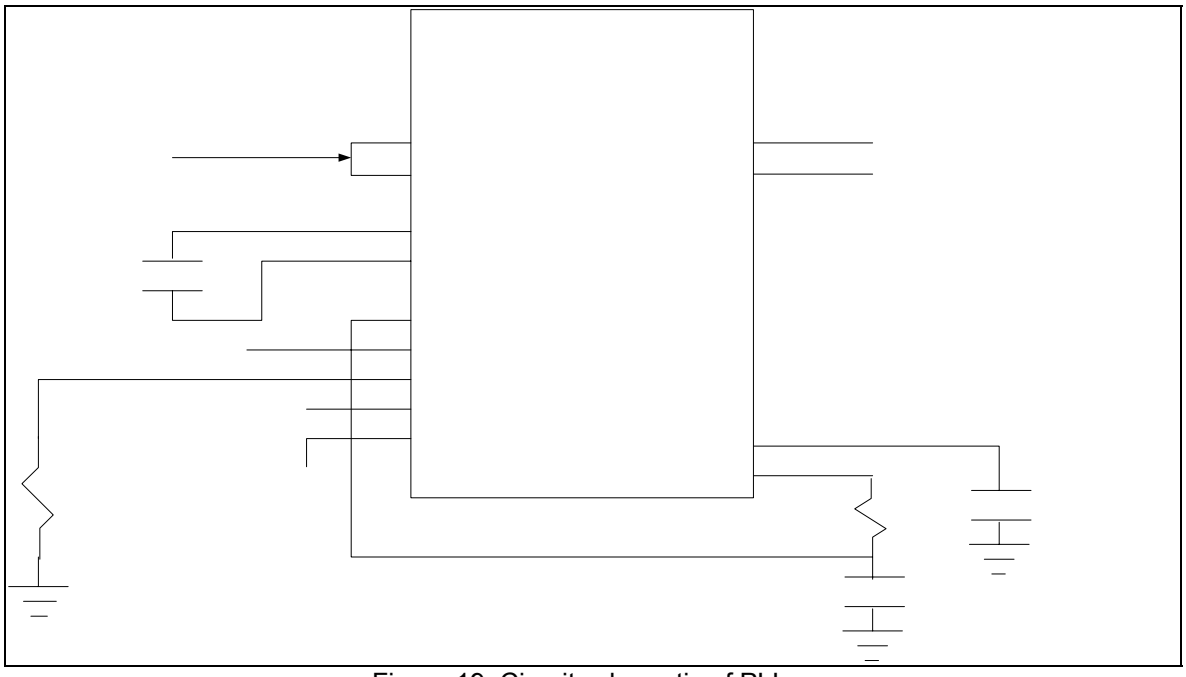

Figure 19: Circuit schematic of PLL

The list of parts that will be used in the implementation is shown in Table 6.

Table 6: Part list for PLL

Part	Value	Specification
R1	220 K	±1%
C1	100 pF	±5%
R2	1.5 K	±1%
C2	100 pF	±5%
C Lock Detect	100 pF	±5%

In this circuit schematic, the values were chosen as follows:

- R1 and C1 were chosen using the data sheet so that the center frequency of the PLL would be 115 KHz (the data rate which is expected to be input)
- R2 and C2 were selected so that the time constant on the lock detect pin would be long enough to keep lock between transmissions
- C Lock Detect was chosen to keep the lock output high between transmissions
- Pin 10 was left as a no connect because the input is already demodulated
- Pin 12 was left as a no connect because if the input resistance on pin 12 is infinite (open circuit) the PLL will operate with no offset frequency – exactly as desired.

Vco voltage – for debugging

C1

No Connect – Demodulation not used

No Connect – So no offse frequency is present

Signal Inp

R1

2.2.6 FPGA

The purpose of the FPGA is to recognize the header signal, peel off the input data for the DUT (which will follow the header signal) and send the input data to the DUT. The FPGA will have the correct clock signal for the data it receives from the PLL, and the header for each packet of data will be 101010101010 (The shift register on the transmit side sends a constant header – refer to Section 2.2.3 for details). The FPGA code will be such that on each rising clock edge (when the clock input goes from 0 to 3 volts) the FPGA will read the value of the input signal and shift it into a register 16-bits long. Whenever the FPGA reads in 101010101010 it knows that it has just read a header signal and will gather the next 4 bits (the inputs to the DUT from the Teradyne J750) and output them simultaneously to the DUT. In this way, the inputs from the J750 are recreated exactly on the DUT side. A block diagram of the FPGA is shown in Figure 18.

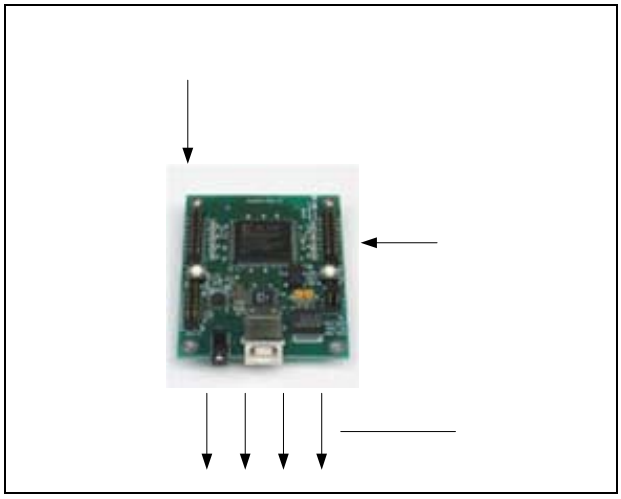

Figure 20: Block diagram of FPGA

The team has chosen to use the Altera Educational Institution Development Board and FPGA. The FPGA is already mounted on a PCB and the team has been given the FPGA and PCB setup from the department to use for the duration of the project (the setup is used in CprE 305 classes and the department allowed the team to use a spare one).

The code for the FPGA that will read the input data, recognize the header signal and pass the input signals to the DUT is shown on the next page.

```
module shiftreg(CLK, indata, outreg);
input           CLK, indata;
output          [7:0]outreg;
reg[11:0]       tempreg;
reg[7:0]        outreg;
reg                     clear;


always @(posedge CLK)
        begin


        if(clear==1)
                begin
                tempreg = 12'b000000000000;
                clear = 0;
                end
        else if(tempreg[11:8] == 4'hA)
                begin
                outreg = tempreg[7:0];
                clear = 1;
                end
        else
                begin
                tempreg[11:1] = tempreg[10:0];
                tempreg[0] = indata;
                end

        end
endmodule
```

Basically, the code shifts in the input data at each rising clock edge and stores the input data in a shift register. When it recognizes that is has shifted in a header signal (101010101010), it outputs the following 4 input bits. The timing simulation for the code is attached in Appendix A with a short explanation of its meaning.

2.2.7 DUT

The purpose of the DUT is to receive the input signals, function as it should, and deliver output signals to the output shift register so that they can be sent back to the Teradyne J750.

The team has chosen to use the Texas Instruments SN74LVC2G74 Single D flip-flop for the initial test. Its data sheet is attached in Appendix D. The device was chosen because it has 4 input signals (clock, D, preset and clear), 2 outputs (Q and Q bar) and its operation is simple and well-understood. After the system is shown to work for such a simple DUT, it will be easy to expand operation to more complex DUTs. The circuit schematic for the DUT is shown in Figure 21 on the next page.

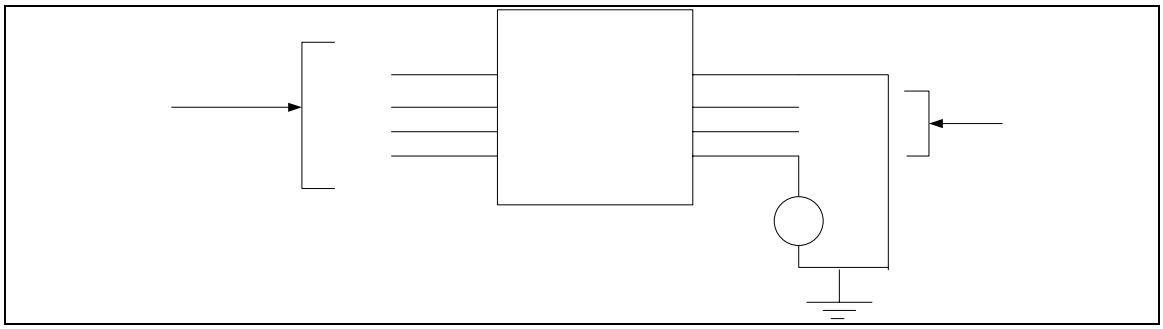

Figure 21: Circuit schematic of D flip-flop

A sample set of inputs and outputs is shown in the waveform diagram in Figure 22.

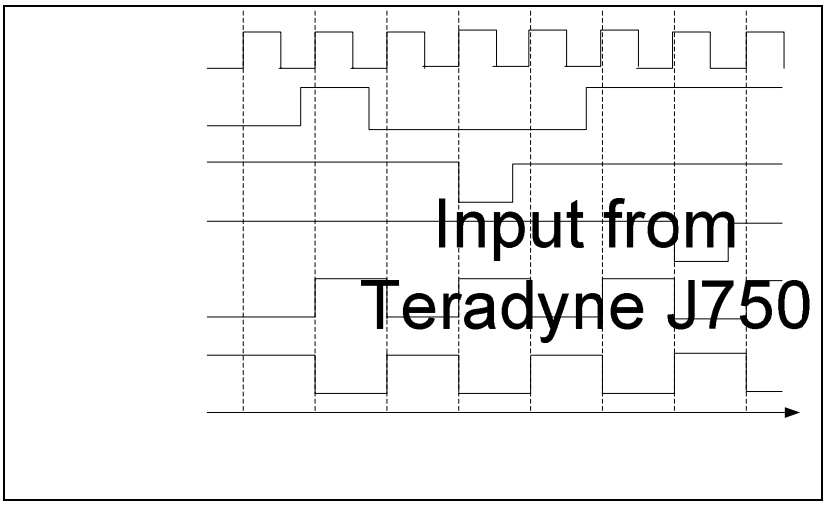

Figure 22: Timing diagram of D flip-flop

Notice that Q bar is always the inverse of Q. Also, the output Q follows D on every rising clock edge, unless prebar sets Q to 1 or clear sets Q to 0. This test pattern could be generated by the Teradyne J750 (see section 2.2.2 for information on generating input signals using the J750) the outputs Q and Q bar would be sent back to the Teradyne for viewing, as will be described in the following sections.

2.2.8 Output shift register

The purpose of the output shift register is to take the output signals from the DUT, serialize them and attach a header to them so that they can be sent through the transmitter (the transmitter will only accept serial data).

The same part that was used for the shift register in section 2.2.3 will be used here (Fairchild Semiconductor 74F676PC shift register). For more information on the part and its operation, see Section 2.2.3 or the data sheet in Appendix D. Again, the 16-bit parallel to serial shift register will be used to serialize the two output signals Q and Q bar from the device under test and attach a static header to the packet that will be sent. In this case, there is no PLL on the Teradyne J750 side of the system, so the static header doesn't have to be 101010101010. Instead, the header will be used to make the outputs Q and Q bar easily recognizable and obvious when they are received by the Teradyne J750.

The circuit schematic for this portion of the system is shown in Figure 23.

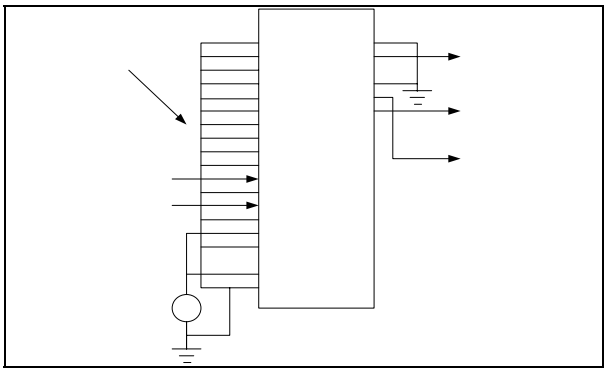

Figure 23: Circuit schematic of the output shift register

The reason for choosing the static header as it is shown will become obvious in Section 2.2.10. The clock pulse and mode select control inputs will be controlled by the FPGA – the FPGA will simply pass the same clock recovered from the PLL to the shift register, and change the mode select such that the data rate output is 115.2 Kbps.

2.2.9 TRM2, wireless connection and RCV2

The purpose of this transmitter and receiver portion of the system is to wirelessly transmit the header and the serialized outputs from the DUT. This portion of the wireless system operates at 914 MHz, so that there will be no interference between the two wireless systems. A block diagram of the system is shown in Figure 24.

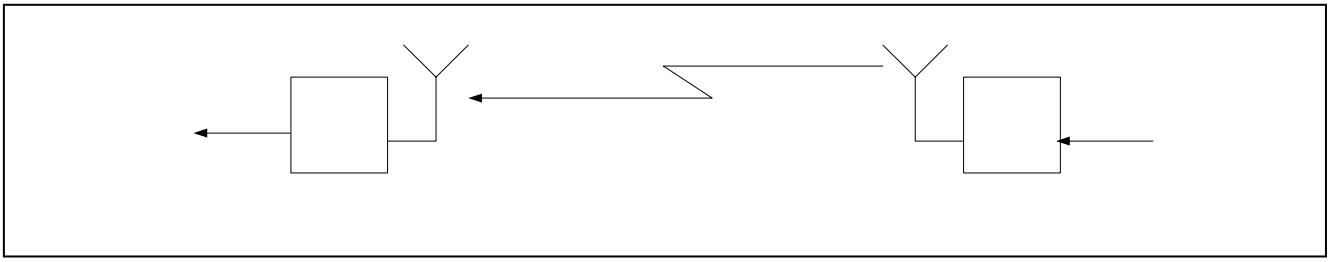

Figure 24: Block diagram of wireless setup TRM2 to RCV2

The group has chosen a transmitter and receiver from RF Monolithics to implement this subsystem. The parts chosen are the TX 6004 (transmitter – TRM2) and the RX 6004 (receiver – RCV2). Their data sheets are attached in Appendix D. They communicate at 914 MHz (to avoid interference with TRM 1 and RCV 1), and Dr. Weber has donated the antennas for both the TX and RX 6004 components. The TX 6004 can transmit data up to 115.2 Kbps and the RX 6004 can receive data at rates up to 115.2 Kbps.

Again, the data sheets for the TX and RX 6004 were used to create circuit schematics that will allow the parts to operate with ASK modulation, and the components used in the external circuitry were also specified in the data sheets for the TX and RX 6004. The circuit schematics and parts are very similar to those used for the TX and RX 6000. The circuit schematic for the TX 6004 is shown below in Figure 25.

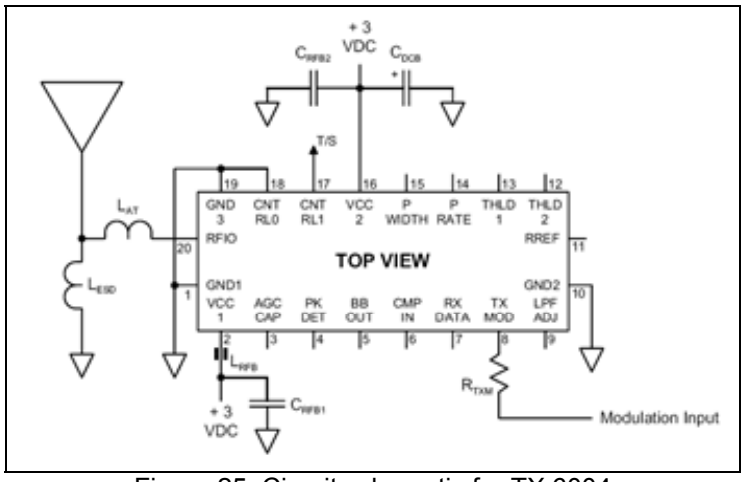

Figure 25: Circuit schematic for TX 6004

Antenn

The parts that will be used to create the circuit (aside from the TX 6004) are listed in Table 7.

Table 7: Part list for TX 6004

Part	Value	Specification
TXMOD Resistor RTXM	6.8 K	±5%
DC Bypass Capacitor CDCB	3.3 µF	±5%, tantalum
RF Bypass Capacitor 1 CRFB1	27 pF	±5%
RF Bypass Capacitor 2 CRFB2	100 pF	±5%
Series Tuning Inductor LAT	10 nH	±5%
Shunt Tuning/ESD Inductor LESD	100 nH	±5%

The circuit schematic to allow the RX 6004 to receive data that has been modulated using ASK is shown in Figure 26.

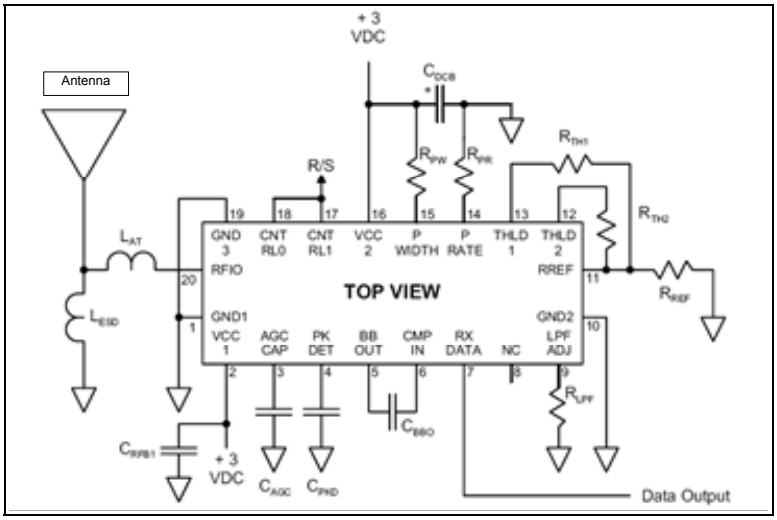

Figure 26: Circuit schematic for RX 6004

The parts that will be used to implement the circuit (aside from the RX 6004) are listed in Table 8 on the next page.

Table 8: Part list for RX 6004

Part	Value	Specification
Capacitor CAGC	2200 pF	±10% ceramic
Capacitor CPKD	0.001 µF	±10% ceramic
Capacitor CBBO	0.0027 µF	±10% ceramic
Resistor RBBO	0 K	±5%
Resistor RLPF	15 K	±5%
Resistor RREF	100 K	±1%
Resistor RTH2	100 K	±1%
Resistor RTH1	10 K	±1%
Resistor RPR	160 K	±5%
Resistor RPW	1000 K	±5%
DC Bypass Capacitor CDCB	4.7 µF	±5% tantalum
RF Bypass Capacitor 1 CRFB1	27 pF	±5%
Antenna Tuning Inductor LAT	10 nH	±5%
Shunt Tuning/ESD Inductor LESD	100 nH	±5%

2.2.10 Teradyne J750 – receive data

The purpose of the receiving side of the Teradyne J750 is to take the serial output from RCV2 and display the waveform on the PC attached to the Teradyne.

The task sounds simple, but there are many steps that must be followed to get outputs into the Teradyne J750 and display them on the PC attached. In order to display an output, one can follow the flowchart in Figure 27.

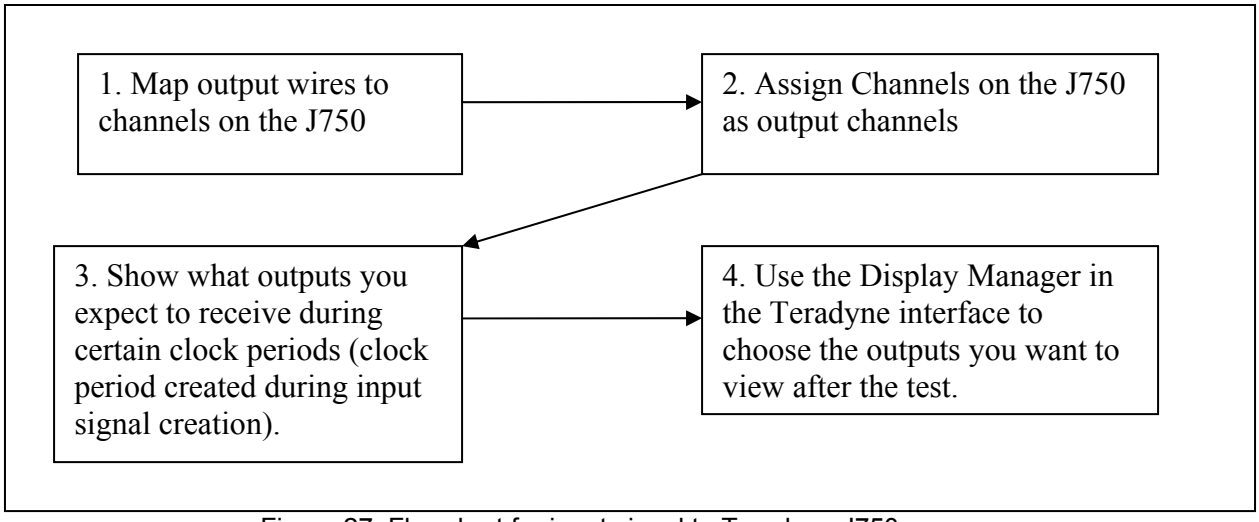

Figure 27: Flowchart for input signal to Teradyne J750

More detailed explanations of the process to view output waveforms are given in the Teradyne J750 manual. However, the team has executed tests and viewed the outputs as part of the preparatory research for the project, and will be able to view the output waveform from RCV2 without problem.

2.2.11 Viewing the output data

In order to understand the output from the DUT sent through the wireless connection, the team must be able to read the waveform that the Teradyne J750 displays. The header attached to Q and Q bar before the outputs are transmitted is used to view the values of Q and Q bar quickly and easily.

The data stream that is sent is as follows (where logic 1 is 3 volts, and logic 0 is 0 volts).

010 (Q) 0 (Q bar) 0000000000

In the above stream (Q) is the bit that represents the value of Q at the moment the data packet was sent, and (Q bar) is the bit that represents the value of Q bar at the moment the data was sent. In order to understand the value of the header, look at the waveforms in Figure 28.

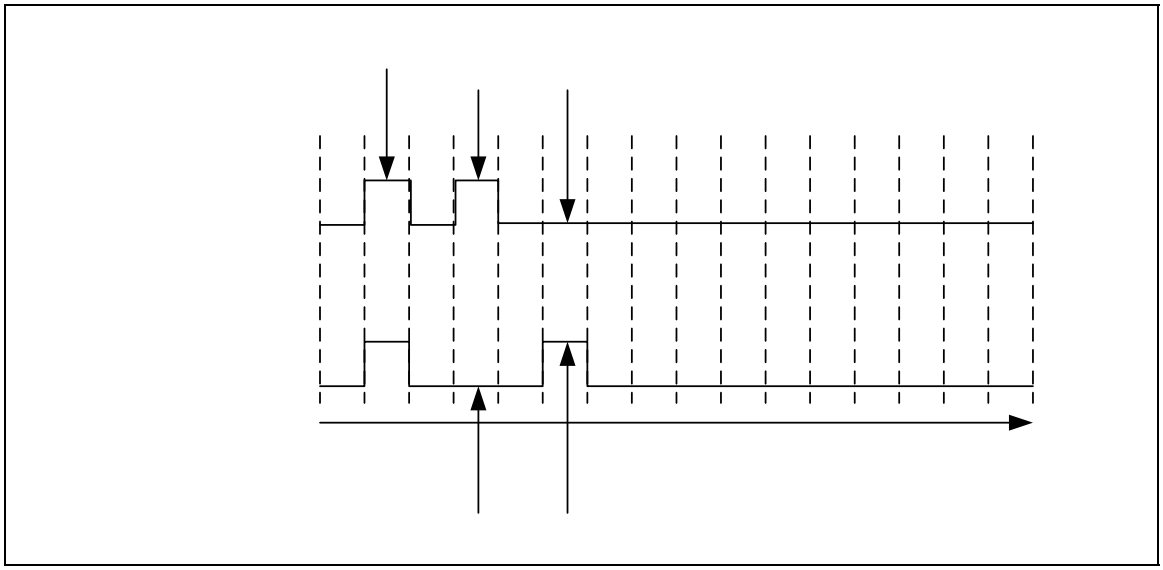

Figure 28: Timing diagram of output waveform

As one can see from the figure, the leading 1 indicates the beginning of a data packet. Two bits after the leading 1 contain the value of Q and four bits after the leading 1 contains the value of Q bar. The ten bits of 0 sent after Q bar are used to create space between packets. The next time a 1 is seen on the output, it is known that the values of Q and Q bar will be seen in the second and fourth bits following the leading 1, respectively.

3. Estimated Resources and Schedules

3.1 Personnel Effort Requirements

The total numbers of hours spent on each task were initially estimated as in Table 9a. These were calculated based on the teams' estimates of hours to be spent on each subtask throughout the semester along with other unforeseen time commitments. As seen below, these were broken down into problem definition, technology considerations and selection, end-product design, end-product prototype implementation, end-product testing, end-product documentation, end-product demonstration, and project reporting.

The initial personnel efforts can be explained as follows. The problem definition was greatly facilitated by the project plan, so the time allotted to finish it was minimal. Technology considerations needed to be researched, and criteria had to be determined and products evaluated. The end-product design was estimated take a large portion of the time. Nathan and Adnan, the Electrical Engineers, were to take a heavier role in this area due to the fact that it involves more circuitry and piecing together of components. The whole team was to take an active part in both the implementation and the end-product testing however Dan and Kyle were to spend a little bit more time coding as they are computer engineers. Kyle has also been the webmaster, which has given him a greater role in the documentation aspect of the project.

Table 9a: Estimated Personnel Efforts

Personnel	**Problem Definition**	**Technology Considerations and Selection**	**End-Product Design**	**End-Product Prototype Implementation**	**End-Product Testing**	**End-Product Documentation**	**End-Product Demonstration**	**Project Reporting**	**Est. Total**
Nathan Gibbs	10 hrs	15 hrs	60 hrs	40 hrs	53 hrs	18 hrs	15 hrs	12 hrs	**223 hrs**
Dan Holmes	10 hrs	15 hrs	45 hrs	60 hrs	55 hrs	20 hrs	10 hrs	12 hrs	**227 hrs**
Adnan Kapadia	10 hrs	15 hrs	60 hrs	40 hrs	56 hrs	20 hrs	10 hrs	12 hrs	**223 hrs**
Kyle Peters	10 hrs	15 hrs	45 hrs	40 hrs	58 hrs	21 hrs	20 hrs	10 hrs	**229 hrs**
Total	***40 hrs***	***60 hrs***	***210 hrs***	***190 hrs***	***222 hrs***	***79 hrs***	***55 hrs***	***46 hrs***	***902 hrs***

The following paragraph will describe the changes to the team's estimated personnel requirements. The updated hours can be viewed as in Table 9b. The main change in the team's revised table is that the documentation hours have already been fulfilled as they were previously estimated. Therefore the initial estimated hours will need to be greatly increased in both the project reporting and the end-product documentation. The team

added Kyle as a greater contributor to the documentation because Kyle has the webmaster responsibilities for the team. The problem definition started off slower than expected as the actual project was not concrete and had changed drastically from the original description of the proposed project. The project definition was given more hours because of this reason. Despite the setbacks, the problem definition is complete. The technology consideration hours have stayed the same and are also complete. The team lowered the end-product design time, as the design is coming together faster than previously expected. It will not be complete however, until the team has a working system. This is due to the fact that the design, implementation, and testing of the project may have to be repeated many times before a working end-product is acquired. Still, the implementation hours will stay the same, as the group allotted for such a cycle in its original estimate. Lastly, Kyle's hours of end-product testing have been lowered to compensate for the greater role in the documentation.

Table 9b: Revised Estimated Personnel efforts

Personnel	**Problem Definition**	**Technology Considerations and Selection**	**End-Product Design**	**End-Product Prototype Implementation**	**End-Product Testing**	**End-Product Documentation**	**End-Product Demonstration**	**Project Reporting**	**Est. Total**
Nathan Gibbs	15 hrs	15 hrs	50 hrs	40 hrs	53 hrs	30 hrs	15 hrs	40 hrs	**258 hrs**
Dan Holmes	15 hrs	15 hrs	40 hrs	60 hrs	55 hrs	30 hrs	10 hrs	30 hrs	**255 hrs**
Adnan Kapadia	15 hrs	15 hrs	50 hrs	40 hrs	56 hrs	30 hrs	10 hrs	40 hrs	**256 hrs**
Kyle Peters	15 hrs	15 hrs	40 hrs	50 hrs	48 hrs	40 hrs	20 hrs	30 hrs	**258 hrs**
Total	***60 hrs***	***60 hrs***	***180 hrs***	***190 hrs***	***212 hrs***	***130 hrs***	***55 hrs***	***140 hrs***	***1027 hrs***

3.2 Other Resource Requirements

The team's other resource requirements were originally thought to be fairly limited. The Teradyne tester was already donated to the Iowa State Campus and was available for use without charge. The team needed to print its project poster and purchase the TI wireless LAN chip and DUT. A summary of the initial resources required is presented in Table 10a.

Table 10a: Estimated additional resources

Item	**Team hours**	**Other hours**	**Cost**
Printing of project poster	12 hrs	0 hrs	$65.00
Teradyne Integra J750 Test System	0 hrs	0 hrs	Donated
TI wireless LAN Chip (x1)	0 hrs	0 hrs	$20.00
DUT	0 hrs	0 hrs	$20.00
Total	**12 hrs**	**0 hrs**	**105.00**

After the technology selection was completed, the team realized that many more parts were needed than originally thought. This can be viewed in Table 10b. Fortunately, most of these parts will be donated by Iowa State University, these items are designated by the letter 'D'. The PCB milling will cost many man-hours as only one team member is familiar with the process. The poster has already been completed, so its cost is actual and all of the transmitter and receivers have been ordered, so their costs are final as well. Thus, the cost of additional resources should not fluctuate much.

Table 10b: Revised estimated additional resources

Item	Team hours	Other hours	Cost
Printing of project poster	12 hrs	0 hrs	$65.00
Teradyne Integra J750 Test System (D)	0 hrs	0 hrs	$500,000
D Flip-Flop (TI- SN74LVC2G74)	0 hrs	0 hrs	$0.43
Transmitter (RF Monolithics TX6000) (D)	0 hrs	0 hrs	$14.00
Transmitter (RF Monolithics TX6004) (D)	0 hrs	0 hrs	$14.00
Receiver (RF Monolithics RX6000) (D)	0 hrs	0 hrs	$20.00
Receiver (RF Monolithics RX6004) (D)	0 hrs	0 hrs	$20.00
4 x 50 ohm antennas (D)	0 hrs	0 hrs	$20.00
PCB milling (D)	30 hrs	0 hrs	$2000.00
FPGA (D)	0 hrs	0 hrs	$200.00
Supplementary circuit components (D)	0 hrs	0 hrs	$15.00
2 x 16-bit shift registers (Fairchild 74F676)	0 hrs	0 hrs	$18.24
Phase-locked loop (TI CD74HC7046A)	0 hrs	0 hrs	$1.23
Total	**42 hrs**	**0 hrs**	**$502,387.90**

3.3 Financial Requirements

The initial cost for the project can be viewed in Table 11a. The calculation assumes that all team members' hourly wage is 11.00 dollars per hour.

Table 11a: Initial estimated project costs

Item	W/O Labor	With Labor
Parts and Materials:		
a. Printing of project poster	$65.00	$65.00
b. Teradyne Integra J750 Test System	Donated	Donated
c. TI Wireless chip	$20.00	$20.00
d. DUT	$20.00	$20.00
Subtotal	$105.00	$105.00
Labor at $11.00 per hour:		
a. Nathan Gibbs		$2,343.00
b. Dan Holmes		$2,387.00
c. Adnan Kapadia		$2,343.00
d. Kyle Peters		$2,409.00
Subtotal		$9,482.00
Total	**$105.00**	**$9,587.00**

The revised estimated project costs are as seen in Table 9b. This estimate includes the updated hours from the team personnel effort table. Listed also are the parts that will be donated and the list of parts that the team will purchase on their own. Many of the parts will be donated by the team's advisor Dr. Robert J. Weber. The FPGA will be donated by the Iowa State Department of Computer and Electrical Engineering. The poster has already been completed and had a cost of approximately $65.00. The need for the TI wireless chip has been erased completely. Instead, the team will use two pairs of transmitters and receivers. Each transmitter and receiver will also need an antenna. The team will purchase the two 16-bit shift registers and the D flip-flop.

Table 11b: Revised estimated project costs

Item	W/O Labor	With Labor
Parts and Materials:		
a. Printing of project poster	$65.00	$65.00
b. Teradyne Integra J750 Test System	Donated	Donated
c. 1 - Transmitter (RF Monolithics TX6000)	Donated	Donated
d. 1 - Transmitter (RF Monolithics TX6004)	Donated	Donated
e. 1 - Receiver (RF Monolithics RX6000)	Donated	Donated
f. 1 - Receiver (RF Monolithics RX6004)	Donated	Donated
g. 4 - 50 ohm standard antennas	Donated	Donated
h. 2 - 16 bit shift registers (Fairchild 74F676)	$18.24	$18.24
i. 1 - FPGA student development board	Donated	Donated
j. 1 - D flip-flop(TI SN74LVC2G74)	$0.43	$0.43
k. Supplementary circuit components	Donated	Donated
Subtotal	$83.67	$83.67
Labor at $11.00 per hour:		
a. Nathan Gibbs		$2,838.00
b. Dan Holmes		$2,805.00
c. Adnan Kapadia		$2,816.00
d. Kyle Peters		$2,838.00
Subtotal		$11,297.00
Total	**$83.67**	**$11,380.67**

3.4 Project Schedule

The figures below are Gantt charts representing the initial expected project schedule and the revised expected project schedule. The schedule has built in a week of slack so if a task takes longer than expected, the team can still complete the project on time. The blue lines represent the initial schedule and the red lines represent the revised project schedule. The black lines inside the red lines represent the actual amount of work completed in that particular field. The breakdown of the revisions is as follows:

Figure 29 is a Gantt chart of the tasks problem definition, technology implementation. The team is very close to being on schedule. The problem definition is done, and the end product design is close to being done. However the schedule has changed from its original state. The team no longer needs to choose TI chips sets. Instead, the team needs to identify and accept transmitter and receiver pairs. The team did not select transmitter and receivers as early as expected because the technology considerations and end product design need to be finalized before parts are ordered. Because the end-product design is so close to completion, most of the parts have been ordered and the team is waiting to receive them.

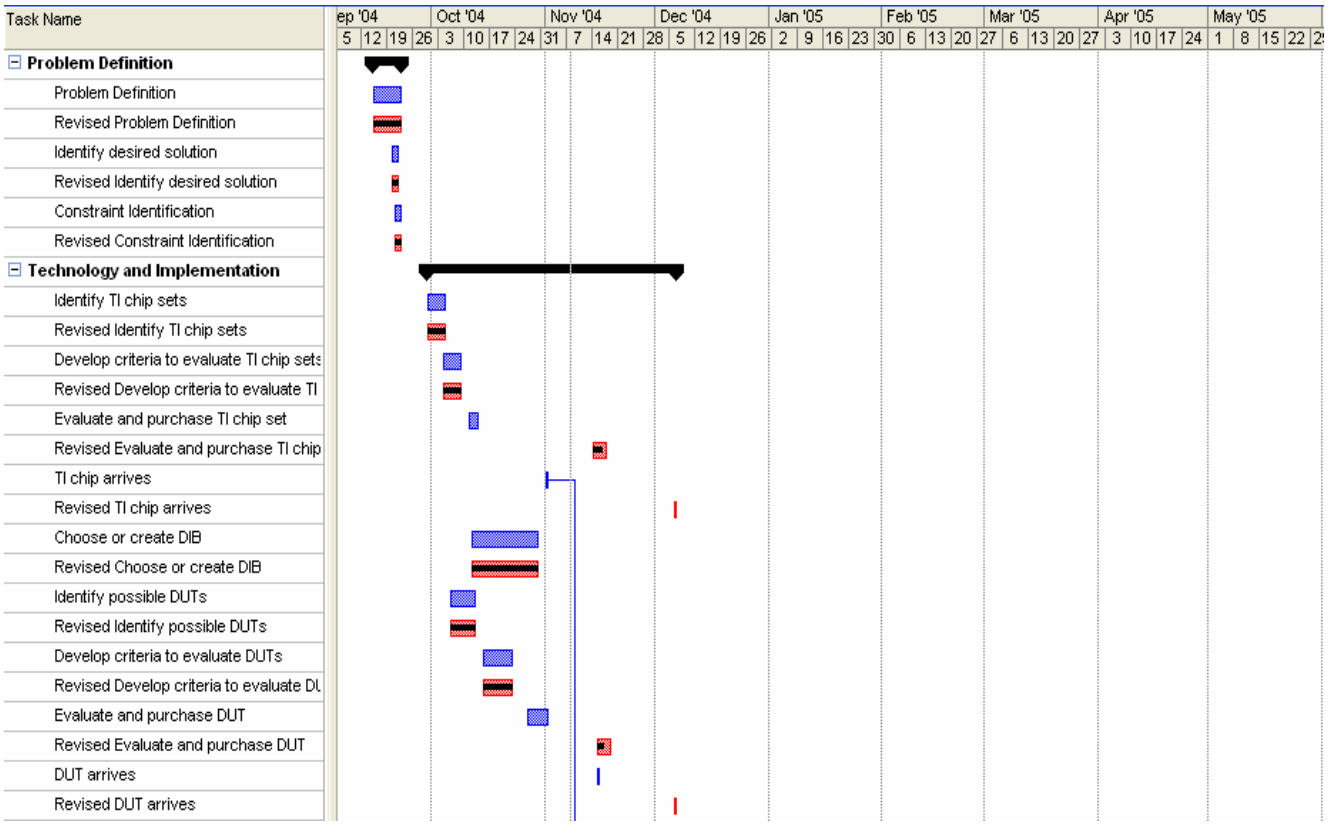

Figure 29: Revised Gantt chart for problem definition and technology implementation

Figure 30 is a Gantt chart of the end product design and the end product implementation. Most of this schedule is the same except that research was done earlier then planned, as the team wanted to research parts before they were ordered. The team also started devising a way that the S/R network will interface with the Teradyne earlier than anticipated.

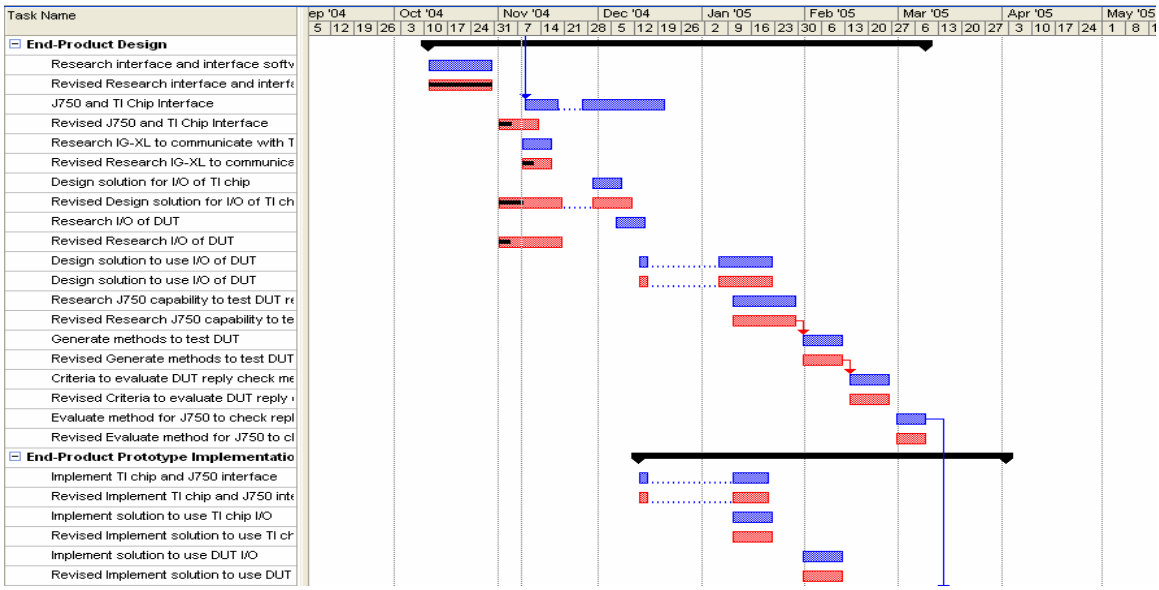

Figure 30: Revised Gantt chart of the end product design and implementation

Figure 31 is a Gantt chart of the end-product testing and the end-product documentation. The initial and revised parts of this chart are exactly the same as the team has gotten its design goals finalized and believes it can stick with its original schedule.

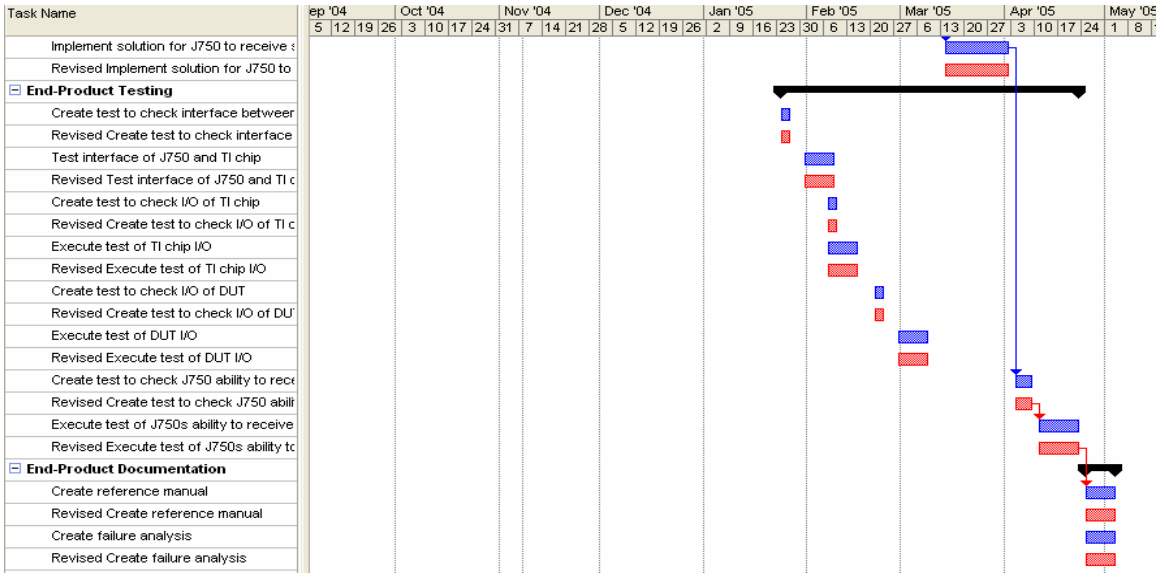

Figure 31: Revised Gantt chart of end product testing and documentation

Figure 32 is a Gantt chart of the end-product demonstration. The revised and initial estimates in these areas remain the same. The team is on schedule in these areas.

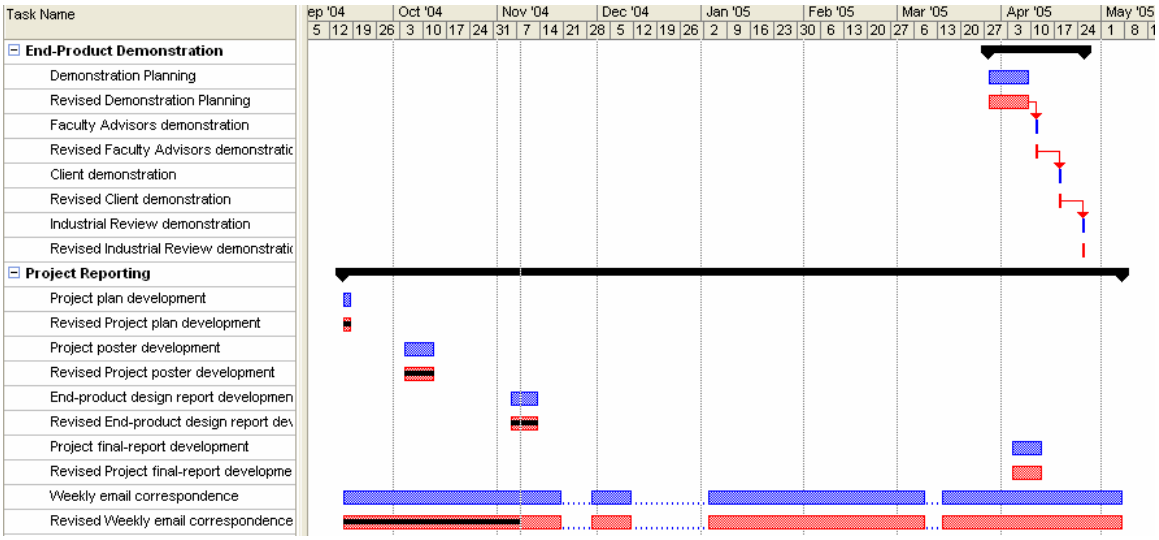

Figure 32: Revised Gantt chart of end-product demonstration

The project deliverables are shown in Figure 33. As you can see from the chart, all initial estimated deliverables are on schedule and the team has completed all of the deliverables up to the current time.

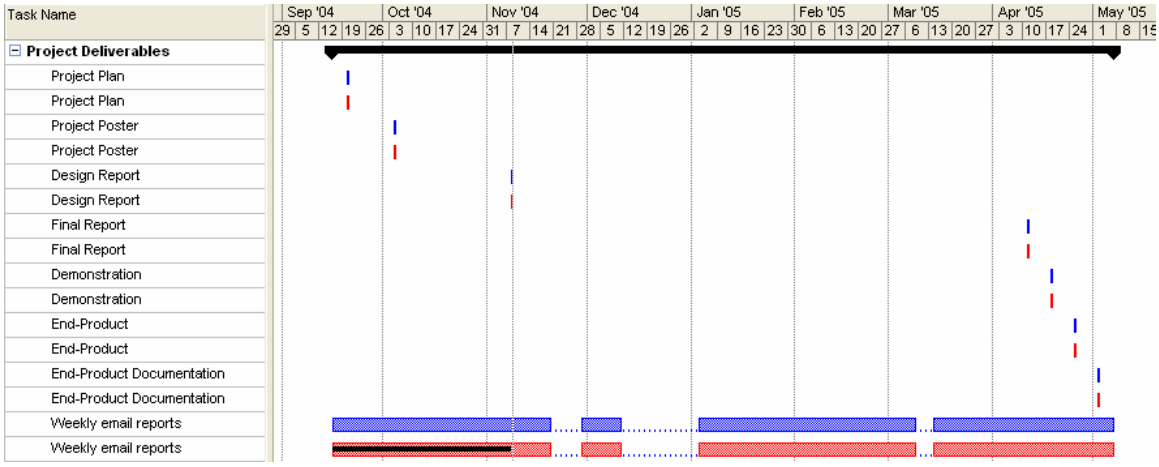

Figure 33: Revised Gantt chart of deliverables

4. Closure Materials

This section provides the client, faculty advisor and team member's information and the closing summary.

4.1 Project Team Information

4.1.1 Client Information

Department of Electrical and Computer Engineering
College of Engineering
Iowa State University
2215 Coover Hall
Ames, IA 50011

4.1.2 Faculty Advisor Information

Dr. Robert J Weber
301 Durham
Ames, IA 50011
Office: (515) 294-8723
Fax: 515-294-1152
weber@iastate.edu

4.1.3 Team Members' Information

The contact information for the members of the project team can be found in table 11.

Table 11: Team member information

Nathan Gibbs **3279 Birch Stevenson** **Ames, IA 50013** **(515) 572-3568** **gibby711@iastate.edu**	**Adnan Kapadia** **126 Beedle Dr. Apt. 206** **Ames, IA 50014** **(515) 451-4786** **adnank@iastate.edu**	**Dan Holmes** **113 State Ave.** **Ames, IA 50014** **(515) 451-7215** **choper@iastate.edu**	**Kyle Peters** **4533 Steinbeck #4** **Ames, IA 50014** **(515) 292-0646** **kylep@iastate.edu**

4.2 Closing Summary

Wireless devices are ubiquitous in society, and every new wireless device must have its RF capabilities tested. The ISU ECpE department would like to use the Teradyne J750 tester to test wireless devices. This project will deliver a solid feasibility study into testing wireless systems using the Teradyne J750 digital circuit tester. The results of this study may deliver a digital wireless system capable of testing RF components and will serve as a supplement to the current capabilities of the J750. Faculty members and students alike will be able to use this system for further research and development for wireless testing.

4.3 References

- Senior Design Team Spring 2004, “Teradyne J750 Tester Cookbook.”, February 2004.
- Teradyne, “Teradyne J750 software manual”, 2003.
- SearchNetworking.com, Radio frequency definitions, September 14th, 2004 <http://searchnetworking.techtarget.com/sDefinition/0%2C%2Csid7_gci214263%2C00.html>.
- Texas Instruments, TRF6901, September 14th, 2004 <www.ti.com.>
- Teradyne, Teradyne J750, September 14th, 2004 <www.teradyne.com>
- Phase-locked loops, November 1st, 2004 <http://www.du.edu/~etuttle/electron/elect12.htm>,