Weekly Report

Date:9/25/13

Group name : Portable FPGA Based Serial Bus Multiplexer (Group 13)
Client/Advisor: Dr. Somani, Dr. Celik
Attendees/Role: Steven LeBlanc - Leader/Firmware Design Adriana Ceylan - Communications/Hardware Design Darin Cleveland - Webmaster/Hardware Design Justin Wheeler - Software Design

Accomplishments For Past Week

What	Who	Date
Very little	Justin	9-25
Finish jtag-Uart/USB to UART workbench and C software to test Nios II Uart system.	Adriana	9-25
Nothing. Busy with career fair.	Darin	9-25
No measurable progress this week	Steve	9-25

Plan for Coming Week/Individual Tasks

What	Who	When
Find out device's vendor and product IDs, refactor USB init code, write testbench for UART both ways, serial->parallel and parallel-> serial	Justin	10-2
Need to load hardware design to FPGA board. Test with C software.	Adriana	10-2
Get laptop working with Altera board. Read and write with PIO. Fix website.	Darin	10-2
Read ChipID from USB controller by reading and writing to registers	Steve	10-2

Pending Issues

Issue	Responsibility
JTAG connections for programming the Nios Have become spotty. Connection will randomly die leaving us with inability to load new firmware	Adriana, Darin, Steve

Individual Hourly Contribution

Darin Cleveland	1
Adriana Ceylan	4
Steve LeBlanc	3
Justin Wheeler	2

Meeting Minutes: 9/25

-All team members should know the hardware and software design of our project comfortably.

-Discussed probability of success and failure related to Dr. Somani's previous senior design projects, and how important it is to keep that in mind.

-Group Tasks: Each team member should draw the software, hardware, and overall structure of our project (in the form of drawings). Within each drawing, each member should know what part of the system they are working on.