Weekly Report

Date:9/18/13

Group name : Portable FPGA Based Serial Bus Multiplexer (Group 13)
Client/Advisor: Dr. Somani, Dr. Celik
Attendees/Role: Steven LeBlanc - Leader/Firmware Design Adriana Ceylan - Communications/Hardware Design Darin Cleveland - Webmaster/Hardware Design Justin Wheeler - Software Design

Accomplishments For Past Week

What	Who	Date
Research how add new components to Qsys and how to connect it to nios II processor	Adriana	9/16
Added Darin's UART component to nios II processor in Qsys.	Adriana	9/17
Typed up several FPGA-side USB initialization functions	Justin	9/17
Worked on communicating with the NiosII's PIO. Unsuccessful.	Darin	9/15-9/18
Set up Central Repository	Steve	9/15

Plan for Coming Week/Individual Tasks

What	Who	When
Test UART-nios II components on DE2 board	Adriana	9/20

Reformat some of the USB functions to be more friendly to the other members of the group. Also, write testbench for UART in Modelsim.	Justin	9/24
Continue working on communicating with board. If communication cannot be achieved, will juggle priorities and work on C code for PIO for others to use.	Darin	9/24
Work on low-level register access with USB controller. Will have successfully written and read back.	Steve	9/24

Pending Issues

Issue	Responsibility
Can't get his laptop to communicate properly with Nios.	Darin

Individual Hourly Contribution

Darin Cleveland	5
Adriana Ceylan	5
Steve LeBlanc	7

Justin Wheeler	3

-9/18 Meeting Minutes:
8:14 - Decided not to use DMA.
-Speech: people forget board architecture. “If you’re not making mistakes, you’re not doing it.” “Draw a block diagram.”
8:19 - What we accomplished. Next week’s goals?
8:22 - Set communication standard.
8:26 - Serial cables - crossed vs null.
8:35 - Darin drew a diagram. Everyone must draw software + hardware diagrams, so we’re all on the same page.
8:40 - Architecture level - register transfer level (RTL) - Quartus can generate RTL diagrams.