Weekly Report

Date:11/6/13

Group name : Portable FPGA Based Serial Bus Multiplexer (Group 13)
Client/Advisor: Dr. Somani, Dr. Celik
Attendees/Role: Steven LeBlanc - Leader/Firmware Design Adriana Ceylan - Communications/Hardware Design Darin Cleveland - Webmaster/Hardware Design Justin Wheeler - Software Design

Accomplishments For Past Week

What	Who	Date
Worked on getting my Ubuntu VM to accept USB input	Justin	11/10/13
Fixed and updated Senior Design Website. Worked on USB read/write commands - still unresponsive.	Darin	11/7/13
Worked on deciphering VHDL USB module to understand how it works and how we can hack into it.	Steve	11/6/13
Work on having a proper uart-sram-nios system/ Hello world test.	Adriana	11/6/13

Plan for Coming Week/Individual Tasks

What	Who	When
Finish activating USB on Ubuntu VM and test USB API	Justin	11/17/13
Get USB controller read/write commands functioning.	Darin	11/17/13
Find a VHDL to Verilog translator	Steve	11/15/13

Finish deciphering VHDL code to determine if there's a way to hack into it	Steve	11/13/13
Help assist Steve, Darin with USB and Justin with testing the USB API. Have a working system Hello world test.	Adriana	11/13/13

Pending Issues

Issue	Responsibility
JTAG connections for programming the Nios Have become spotty. Connection will randomly die leaving us with inability to load new firmware.	Adriana, Darin, Steve
Quartus has become very touchy with removing hardware modules from the hardware solution. We need to find a solution that works, and slowly build off of it, saving copies of our system as we go along.	Adriana, Darin, Steve

Individual Hourly Contribution

Darin Cleveland	6
Adriana Ceylan	7
Steve LeBlanc	8
Justin Wheeler	5

Minutes:

8:05 - Justin gone, sick. Adriana and Steven sick last week.
8:10 - SRAM structure running. USB controller still unresponsive.
8:14 - timing issues causing it? Likely. When working with address bus, timing is critical.
8:18 - Timing through C code is difficult.
8:25 - Looking over USB control signal documentation…
8:30 - Altera's chip scope can be used to scope out signals from the chip.
8:34 - looking over main.c file for USB control. Issues found.
8:45 - how timing breaks down in C/assembly.
8:50 - main.c issues: 0xf needs to be 0xff and the timing of signals needs to be revised.

9:30 - Leave, after much discussion over timing issues.