Weekly Report

Date:11/20/13

Group name : Portable FPGA Based Serial Bus Multiplexer (Group 13)
Client/Advisor: Dr. Somani, Dr. Celik
Attendees/Role: Steven LeBlanc - Leader/Firmware Design Adriana Ceylan - Communications/Hardware Design Darin Cleveland - Webmaster/Hardware Design Justin Wheeler - Software Design

Accomplishments For Past Week

What	Who	Date
Have a working system with SRAM memory. Now I need to add Darin's UART module by making a qsys component.	Adriana	11-17
Work on poster and final presentation	All	11-19
Main.c file now successfully reads from USB controller!	Darin	11-17
Made bootable USB Linux drive, did some (unsuccessful) testing of API.	Justin	11-17
Successful USB Communication through USB controller to 2nd computer using modified VHDL code	Steve	11-18

Plan for Coming Week/Individual Tasks

What	Who	Date
Integrate a working system with Darin's UART module. Once that works, add 16 UARTs to the system.	Adriana	12-4
Complete poster and presentation	All	12-1
Integrate functional VHDL usb controller program	Steven, Darin	12-4

with Nios.		
Install Ubuntu fully on USB drive so that I can use settings I wouldn't otherwise be able to in order to get the API working	Justin	12-4

Pending Issues

Issue	Responsibility
JTAG connections for programming the Nios Have become spotty. Connection will randomly die leaving us with inability to load new firmware.	Adriana, Darin, Steve
Quartus has become very touchy with removing hardware modules from the hardware solution. We need to find a solution that works, and slowly build off of it, saving copies of our system as we go along.	Adriana, Darin, Steve

Individual Hourly Contribution

Darin Cleveland	6
Adriana Ceylan	9
Steve LeBlanc	10
Justin Wheeler	6

Minutes:

8:12 - USB access, both Darin's approach and Steven's are reading properly!
8:16 - Justin: still trying to get linux to get USB privileges, in order to test his API. He can't use ISU linux computers, he needs root access to manually send data through USB.
8:22 - Adriana is integrating Darin's UART.
8:24 - Darin's code: Implementing read-16-bits commands gets nothing, but read-32-bits returns data, even though it's only 16 wires connected. Why? 3-way protocol. Live lock (opposite of deadlock).
8:35 - Adriana: miss wired Darin's UART, knows how to fix, still moving forward.
8:41 - Steven shows up.

8:43 - Steven’s VHDL USB code is working. Wasn’t before because he didn’t understand VHDL. He knows how to use it now, just not how it works. It is more “complete” and functional than Darin’s main.c file, so focus will be diverted exclusively to the VHDL code integration.
8:49 - Not much is going to get done over the holiday.
Slides: include what we learned. Don’t put it on our poster. In slides, put in example pieces of code to tell example stories about the challenges we faced.