Ultrasound Brain Imaging

INTRODUCTION

The goal of this project was to expand upon a previous group's design for a pulse echo ultrasound system for brain imaging which could be used as a low cost alternative to fMRI. The group was tasked with designing a transmit receive board which could be scalable up to 512 transmit/receive channels.

The objective of the project was to design and implement a working 8-channel transmit/receive board. The transmit circuit will be able to send high voltage pulses (+/-50V) over 8 channels. The design also needed to be easily scalable to up to 512 channels. The receive circuit will then receive the signals from the transducer and amplify them before sending them to a computer interface. This computer interface will also be responsible for controlling the pulses sent to the transducer, though it was not within the scope of our design. The group also designed a protection circuit to limit the voltage amplitude of the signals reaching the computer interface.

REQUIREMENTS

- Send +/- 50 V pulses
  - Voltage needed to excite the transducer
- Operation frequency of ~1 MHz
- Transmit over 512 channels
  - Requirement for the final system
  - Our goal is to design an 8 channel board which can be easily expanded as needed
- Receive over 512 channels
  - Requirement for the final system
  - Our goal is to design an 8 channel board which can be easily expanded as needed
- Total Gain of 70 dB
- Able to connect to the NI computer interface
- Limit input to NI computer interface
  - Maximum input of 2 V_{pp}

GROUP DEC13-01

Client | Advisor

Dr. Bigelow

MEMBERS

Zach Bertram (EE)

Michael McFarland (EE)

Maurio McKay (EE)

Jonathan Runchey (EE/Physics)

BEAMFORMER (LM96570)

- Provides a serial interface to program the high voltage pulser
- Reduces required input channels to control pulser from 18 to 9 digital channels

HIGH VOLTAGE PULSER (LM96550)

- Sends +-50V pulses to the transducer
- Operates at 1 MHz

T/R SWITCH (TX810)

- Protects receive circuitry from high voltage pulses
- Output voltage limited 2 V_{pp}

TRANSDUCER

- Custom 512 linear array
- Converts high voltage pulses (+/-50V) to ultra sonic waves to transmit into the body

LOW NOISE AMPLIFIER (LMH6622)

- High Gain Bandwidth (160 MHz)
- Low noise floor (1.6nV-Hz^1/2)
- Two stage configuration with a gain of 40 dB

OP AMP PROTECTION CIRCUIT

- Limit output voltage to 2 V_{pp}

NI-5752 MODULE

- 32 Analog receive channels
- Contains TI-AFE 5801 analog front end
- Variable gain range –5 dB-31 dB
- 12-bit A/D converter
- Maximum acceptable input 2 V_{pp}

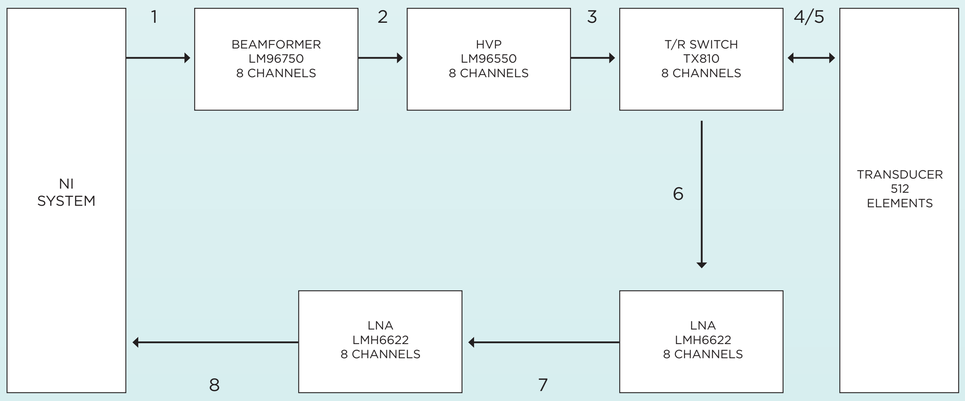

FIGURE 1 DEVICE LAYOUT:

The figure to the left depicts the signal flow through the final system layout. The numbers above the arrows represent the order of signal propagation through he system, while the number in parentheses represent the number of boards needed to obtain a 512 channel design.

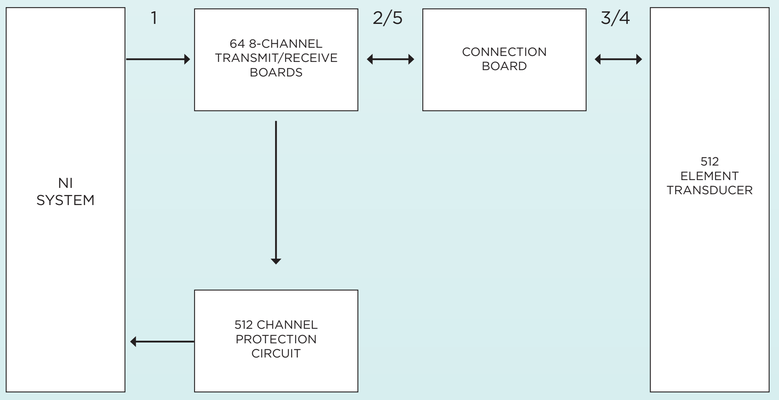

FIGURE 2 BOARD INTERCONNECTIONS:

This figure depicts the multi-board scheme used in the design. The group decided to use a multi-board design to reduce individual board complexity and to allow the client to more easily expand the number of channels at a later date.

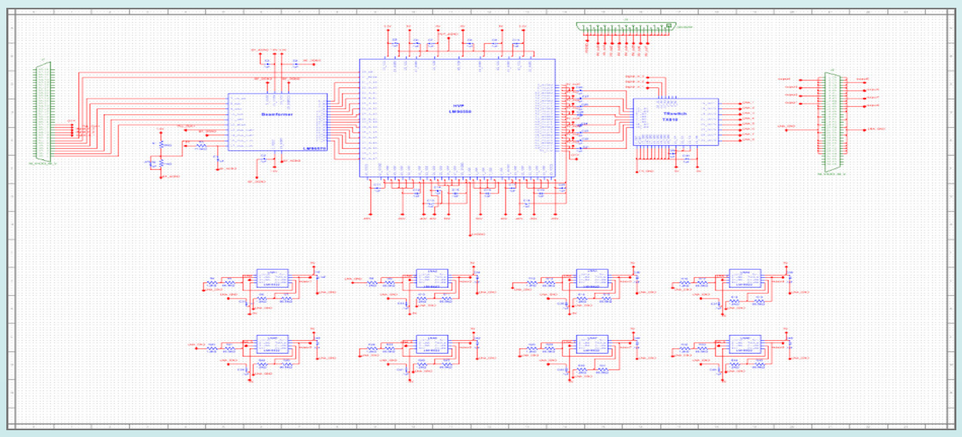

FIGURE 3 8-CHANNEL TRANSMIT RECEIVE SCHEMATIC:

The figure to the left is the schematic for our 8 channel transmit receive board. The ICs included on this board are as follows; LM96570 (Beamformer), LM96550 (High voltage pulser), TX810 (Transmit and receive switch), and the LMH6622 (Low noise amplifier) chip.

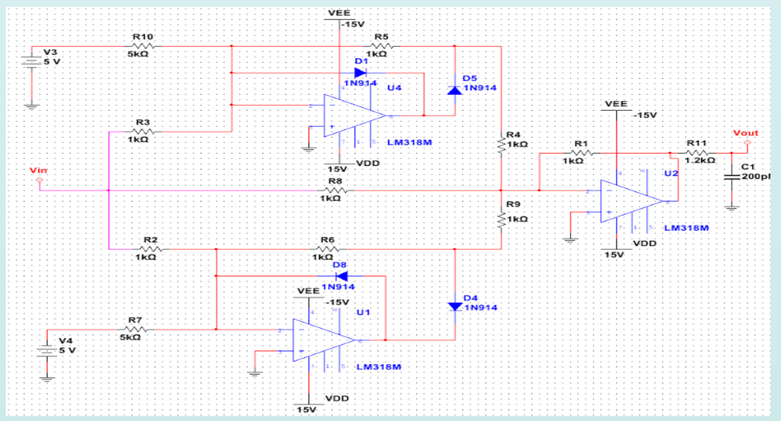

FIGURE 4 PROTECTION SCHEMATIC:

This is the schematic for the protection circuit we will be using to limit the input to the NI computer interface to 2Vpp. This schematic shows the design for only one receive.

CHALLENGES

- Poor documentation from previous group
- Some parts selected by previous group were untested and did not work
- Couldn't easily test complicated SMT parts by simulation or with a breadboard
- No previous experience soldering high pin density SMT parts
- High individual IC costs
- No group members had previous PCB design experience
- No easy way to divide PCB design work among group members

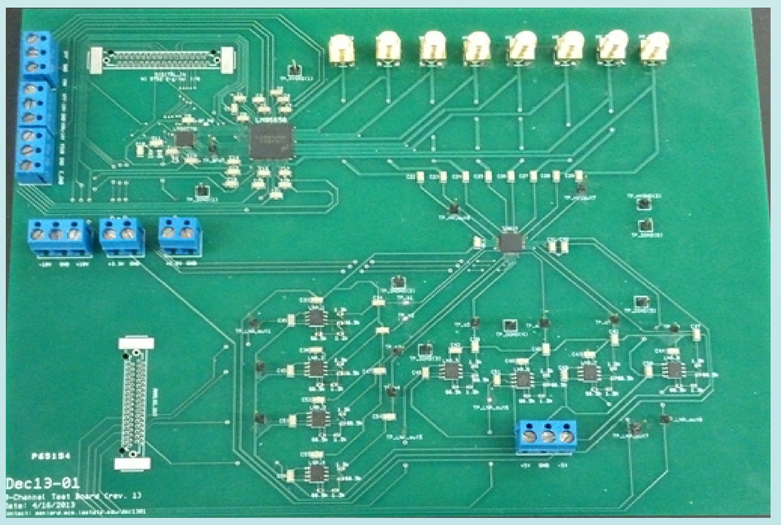

FIGURE 5
Implemented PCB