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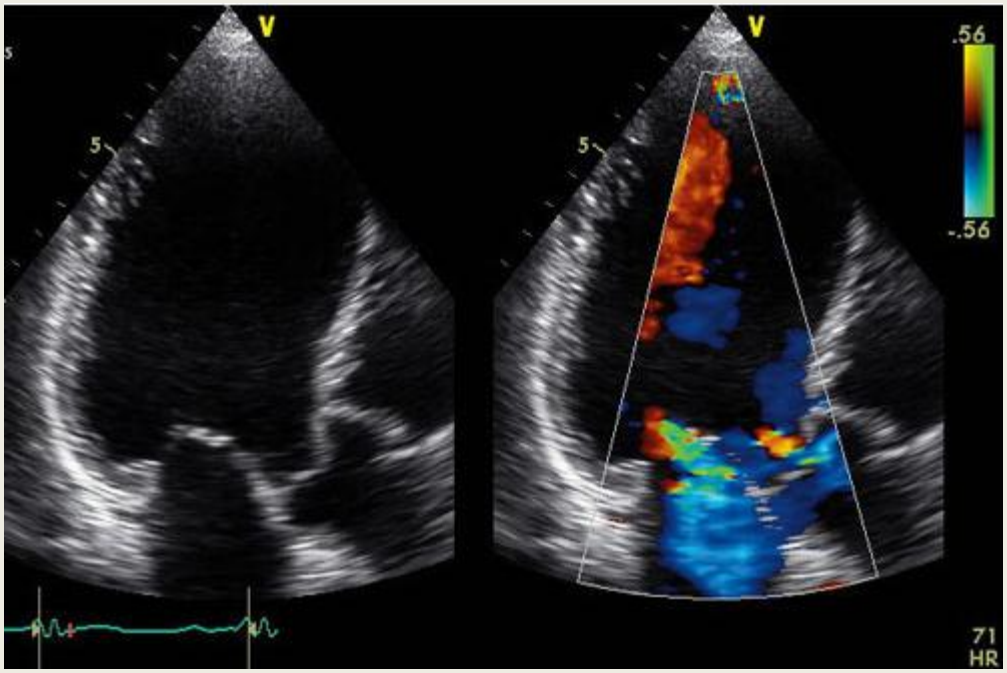
Dr. Tim Bigelow

# Design of a Pulse Echo Ultrasound System




http://www.gehealthcare.com/euen/ultrasound/products/cardiovascular/vivid-q/index.html

Dec2012-04 | Allen Kellar, Amairani Tapia, Francis Ferrer, Justin Batcheler, Jon Driggs, Richard Page

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# Table of Commonly Used Terms

| Term | Meaning |
|---|---|
| "Pulser" | A device that can provide square wave pulses |
| "High Voltage" or "HV" | A voltage level ranging form 20V to 100V |
| "Analog Front End" | A device made by Texas Instruments that incorporates all the necessary hardware to recover ultrasound signals into one package. |
| "Multiplexing" | Switching a small number of inputs amongst a larger number of outputs |

## Problem Statement

In order to understand the project, a brief description of brain-imaging technology will be given. One technology that will be evaluated is fMRI. Functional magnetic resonance imaging (fMRI) is a noninvasive test that uses a strong magnetic field and radio waves to look at blood flow in the brain and detect areas of activity. Oxygen-rich blood and oxygen-poor blood have a different magnetic resonance. The most active areas of our brain receive more oxygenated blood. The advantage in fMRI is that it does not emit radiation like X-rays, computed tomography, and positron emission tomography scans. Although the fMRI is a very effective brain-imaging system, it is also very expensive. In lieu of such high costs, the design of a pulse echo ultrasound system was pursued. A pulse echo system consists of a transducer assembled with 128 small individual elements that can each be pulsed separately. The purpose of pulsing each element separately is to create a phased-array of signals. The phased-array (signals with different phases ranging from 10ns to 20us) will be sent through the ultrasound probe. Additionally, pulse echo ultrasound millions of pulses and echoes are sent and received each second. These sound waves are reflected back to the probe once a boundary between tissues is found, and the reflected signals can be processed to form an ultrasound image.

An ultrasound circuit is composed of many parts that serve different functions. The design that is being used has eight major components that define the circuit. The components are as follows: waveform generator, high voltage amplifiers, transmit/receive circuit, ultrasound transducer, low-noise amplifiers, and variable-gain amplifiers. A block diagram of the system is shown below in Figure 1 where you can see the relations of the components.

## System Description

The goal of the project is to design an ultrasound system that consists of 128 independently accessible channels. The phase of each channel must controllable to roughly 5 nanoseconds. Each channel will also have TX (transmit) and RX (receive) capabilities. Short "Tone bursts" with different phases will be transmitted through an amplifier stage and the received message will pass through an amplifier stage whose gain increases over time. Also the TX stage will need a "blocking" circuit to keep the received message from propagating into the TX circuit. The system will also need to communicate with a pc for data acquisition. The computer interface will also be used to set the phase and amplitude of each channel output.

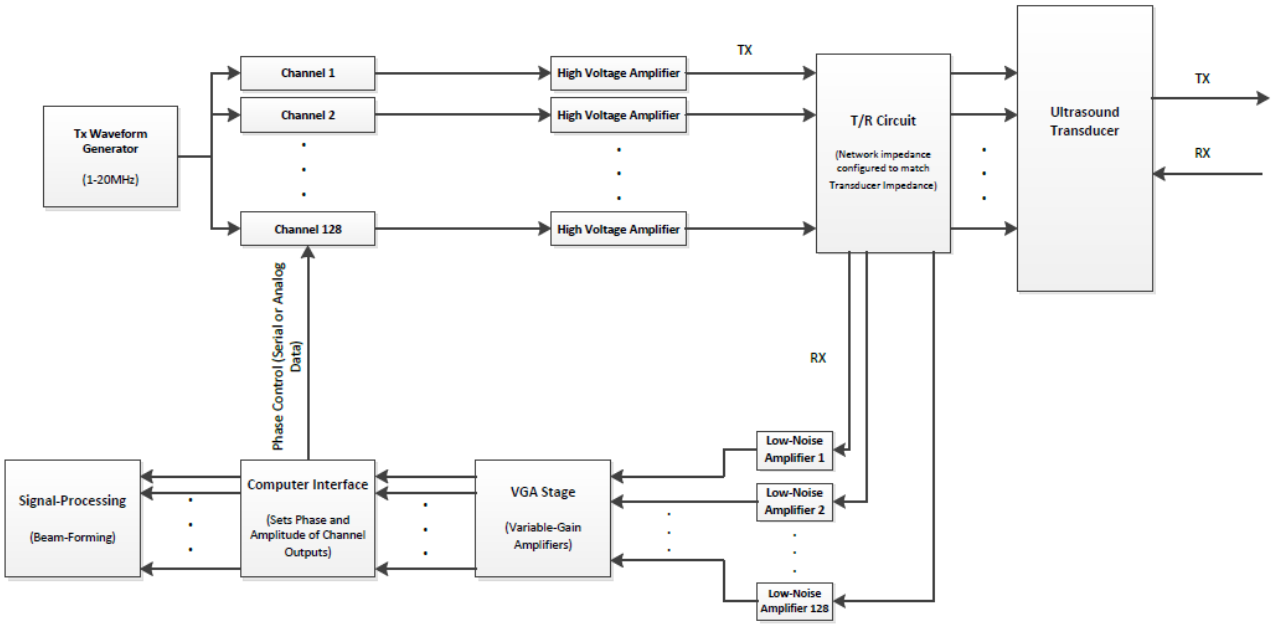


**Figure 1 - Block Diagram of the Ultrasound System**

### Waveform Generator

The waveform generator creates pulses that are used to transmit the ultrasound signal. There are 128 pulses that are being sent to the transmit/receive circuit. The frequency of the system will be 3 MHz due to beam forming technology.

### Analog Front End

The analog front end is a combination of a voltage controlled amplifier and an analog-to-digital converter. The voltage-controlled amplifier contains low noise amplifier, programmable gain amplifier, and voltage-controlled attenuator

### Transmit/Receive Circuit

The transmit/receive circuit will transmit the amplified pulses to the ultrasound transducer. It will receive the reflected low voltage signals from the transducer and use them for the signal processing of the ultrasound.

**Computer Interface**

A computer interface will be used to control the phase and magnitude of the waveform generator channel outputs. The minimum delay is around 5.6 ns. Additionally, reflected signals will be sent to the computer interface for signal processing and recovery.

**Time Delay Blocks**

The time delay blocks on each channel will allow for the user to program a specific time delay into each channel. This functionality allows for the user to program in a specific pulse pattern that will be transmitted through the ultrasound transducer.

**Signal Processing**

Reflected ultrasound pulses will be amplified and communicated to the computer interface for digital signal processing and imaging. All signal processing will be done in the computer interface.

**Transducer**

The transducer, otherwise known as the probe, is the component in the system that has contact with the body. The transducer would receive an electrical pulse and, that pulse would make it vibrate to the determined frequency. Returning sound waves would vibrate the transducer and cause it to emit electrical pulses back into the system to be imaged.

## Operating Environment

The ultrasound system, when completed, will be used by Iowa State University researchers in the Biomedical lab located on the first floor of Coover. Therefore, the physical operating environment of the ultrasound device will not be demanding. There are also no requirements that limit the size or power consumption of the ultrasound system at this point.

## User Interface

In order to ensure that the researchers can use the system effectively for brain imaging, the ultrasound circuit must have a flexible interface to the computer for configuration. Examples of parameters that will need to be configured through the user interface are: each of the 128 channels will have a fully programmable time delay element, the pulse generation circuit must be controlled by the user interface, and the reflected ultrasound pulses must be successfully transferred to the computer interface. Adding such programming functionality adds significant complexity to the circuitry of the system, and also requires that a equally-complex software

interface be created to control the system. However, our team will only be concerned with the hardware aspects of the system.

## Deliverables

**128 Channel Ultrasound System**

For this project, our final expected product will be a 128 channel ultrasound imaging system. The development of this system will be based on extensive research of existing patents on ultrasound imaging circuitry. The ultrasound system will be based on traditional beam technology and used for brain imaging. A transducer will be placed to the temple, on the side of one's head, and the system will communicate with a PC for imaging.

The project will be broken into portions. The first major deliverable will be a simulated 1 channel ultrasound system verified with the PSPICE simulator. From this point a 128 channel system will be designed, simulated, and verified. A 128 channel printed circuit board will be ordered and tested with a PC to show that traditional ultrasound imaging is possible.

**Documents**

PSpice Model: The simulated system will be prepared in PSpice.

Design Document: This document will provide detailed information on the operation and performance specifications of the device. Also, it will include information and requirements on the different integrated circuits that are included in the ultrasound system. Testing and evaluation strategies will be covered, as well.

## Resource requirements

The technical requirements, system requirements, and user interface requirements are given in the tables below.

**Table 1 - Resource Requirement Descriptions**

| System Component: | Requirement Description: |
|---|---|
| Waveform Generator | The waveform generator shall be capable of controlling the pulser integrated circuits in order to produce high-voltage signals. Each output must be individually controllable in order to implement a phased-array system. |
| Waveform Generator | The waveform generator shall be capable of being controlled by the user interface. |
| | |
| High Voltage Amplifier (Pulser) | The high voltage amplifier shall be capable of amplifying the input waveform so the output has a pulse amplitude 190 Vpp. |
| High Voltage Amplifier (Pulser) | The amplifier circuit shall have a bandwidth that exceeds 3 MHz. |
| | |
| T/R Circuit | The T/R circuit shall function as protection against high-voltage transients for the receiver. However, the T/R circuit shall allow high-voltage transmitted signals to propagate to the Ultrasound Transducer. |
| T/R Circuit | The T/R circuit shall only allow a signal with maximum amplitude of X V to enter the receiver circuit. |
| T/R Circuit | The T/R circuit shall have impedance matching with the Ultrasound Transducer. (Note: Ultrasound Transducer Electrical Characteristics are unknown at this point) |
| | |
| Analog Front End | The Analog Front End shall contain a low-noise amplifier to recover a small-magnitude signal from the transducer output. |
| Analog Front End | The Analog Front End shall contain a variable gain amplifier with an adjustable gain. |
| Analog Front End | The Analog Front End shall contain an ADC capable of sampling at 50MSPS and that produces serial LVDS data at the output. |
| | |

| | |
|---|---|
| Transducer | Operates in the 3 MHz frequency range |
| Transducer | Linear array with 128 elements |

## Market and Literature Survey of Similar Products

Ultrasound technology has quickly advanced in the past 20 years due to the introduction of high-power processing and cheaper, more complex integrated circuit components. Modern ultrasound systems are designed by companies with very experienced teams of engineers who rarely share proprietary design information. Therefore, our team began our project by researching how an ultrasound system works at a system-level. Once the overall functionality of the system was understood, we searched for existing patents on individual functional blocks of the system. Useful information was found for: High-voltage pulse generation, transmit/receiver circuitry, digital beam forming, and reflected signal recovery (see the block diagram for reference of the system components listed). Additionally, our client Dr. Bigelow provided us with a product guide from a existing ultrasound system that lists some of its technical specifications (such as minimum time delay and peak waveform amplitude).The technical specifications we gathered from the product guide were incorporated into our project requirements.

Several patents and research papers that have been referenced extensively are given below.

[1] Koen, Myron. "Ultrasound Transmitter." *United States Patent Application Publication* May 6, 2010. 1-9. *United States Patent Database*. Web. 2 Feb 2012.

[2] Udpa, Satish. "Apparatus and Method for Driving an Ultrasonic Transducer." *United States Patent Application Publication* June 3, 1997. 1-9. *United States Patent Database*. Web. 2 Feb 2012.

[3] Camacho, Jorge, and Carlos Fritsch. "Protection Circuits for Ultrasound Applications." *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control* 55.5 May 2008. 1160-1164. *IEEE.* Web. 5 Feb 2012.

[4] Hatfield, J V, P A Payne, and N R Scales. "Transmit and Receive ASICs for an Ultrasound Imaging Multi-Element Transducer." *IEEE* (1994): 1-9. *IEEE*. Web. 13 Feb 2012.

[5] Poulsen, Jens. "Low Loss Wideband Protection Circuit for High Frequency Ultrasound." *IEEE Ultrasonics Symposium* 823-826. *IEEE*. Web. 13 Feb 2012.

## Pending Issues

There are some problems obtaining technical requirements for the ultrasound transducer. Companies, such as Sound Technologies, Inc. and Phillips Healthcare, require their product to be purchased to know the specifications or even speak with an engineer. Therefore, an ultrasound transducer within the project's budget is still being sought for purchase. A similar problem is also faced with the evaluation board. The DSP EVM boards needed require built in DACs and ADCs on the board. We are in contact with Texas Instruments and they are currently assisting us with finding a suitable board among their products.

## Estimated Costs

**Table 2 - Estimated Cost of Hardware**

| Part Number: | Part Description: | Cost: |
|---|---|---|
| ML605 Evauluation Kit | XLINX FPGA Board | $2,063.75 |
| AFE5808EVM | Analog Front End<br>Analog to Digital Converter<br>Evaluation Board | $305 x 4 = $1,220.00 |
| TSW1250EVM | Analysis system | $700.00 |
| TX810 | Transmit/Receive Switch | $11.15 x 4 = $44.60 |
| HDL6V5581 | HV Pulser | $12.75 x 6 = $76.50 |
| MAX14803CCM | High-Voltage Switch Bank | $26.91 x 10 = $269.10 |
| Ultrasound Probe | | Tentative - $3,000.00 |
| *Can be found in design document | Power Electronics | Tentative - $330.00 |
| **Total Cost:** | | **Necessary Hardware Only: $5,783.95**<br><br>**With Evaluation Modules: $7,703.95** |

The table above lists the hardware that is to be purchased for the ultrasound prototype. In order to reduce costs and development time, we have chosen to implement a 32-channel system and multiplex the 128 outputs of the ultrasound probe to the system using a MAXIM high-voltage switch bank.

Feedback from the client is necessary before planning to purchase the evaluation boards for the DSP and data-converters. Once approval is given, the parts will be purchased in order to test the functionality of the waveform generation system.

**Table 3 – Hours Worked**

| Hours Worked (as of 4/16/2012) | |
|---|---|
| **Allen Kellar** | 88 |
| **Amairani Tapia** | 91 |
| **Francis Ferrer** | 94 |
| **Justin Batcheler** | 87 |
| **Jon Driggs** | 135 |
| **Richard Page** | 96 |
| **Total** | 591 |

## Project Schedule

The project will take place over the course of two semesters. During the first semester, the main focus is on project planning and design. We would like to have a working simulation by the end of the first semester. During the second semester, our focus will shift to testing our engineered circuit. The following dates provide a timeline for the schedule we would like to follow.

**Table 4 – Project Schedule**

| Task | Task Detail | Start | Finish | Duration | % Complete |
|---|---|---|---|---|---|
| Problem Definition | Meet w/ advisor; Gain understanding of the project. | 1/9/2012 | 1/13/2012 | 4 Days | 100% |
| Research | Research patents on ultrasound systems. | 1/16/2012 | 2/17/2012 | 32 Days | 100% |

| | | | | | |
|---|---|---|---|---|---|
| Identify Circuit Components | Research components and different technologies; Select components that will be used. | 2/1/2012 | 3/30/2012 | 59 Days | 100% |
| Initial Design | Design 1 channel circuit | 3/1/2012 | 4/9/2012 | 40 Days | 100% |
| PSPICE Simulation 1 | Test and verify via available model files to ensure expected functionality. | 3/15/2012 | 4/20/2012 | 36 Days | 100% |
| Final Design | Expand the 1 channel circuit into 32 channels and implement switching scheme. | 4/9/2012 | 4/27/2012 | 19 Days | 90% |
| Order Parts | Order selected components and printed circuit board | 4/2/2012 | 6/1/2012 | 60 Days | 60% |
| PCB Test Plans | Create test plans for the physical implementation of individual components. | 4/16/2012 | -- | -- | 25% |
| PCB Testing | Test the individual components, and the components combined. | -- | 10/1/2012 | -- | 0% |
| Fabricat Final PCB | Build the final PCB after completed testing. | 10/1/2012 | 10/29/2012 | 29 Days | 0% |

## Project Team Information

**Client and Faculty Advisor Information**

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**Student Team Information**


| | | |
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