PULSE ECHO ULTRASOUND SYSTEM DESIGN



Member Information

- Client and Faculty Advisor Information
 - Dr. Timothy Bigelow, <u>bigelow@iastate.edu</u>
- Student Team Information
 - Jon Driggs Team Leader
 - Francis Ferrer Team Leader
 - Allen Kellar Communications
 - Amairani Tapia Communications
 - Justin Batcheler Web Designer
 - Richard Page Web Designer

Brain Imaging Technology

- fMRI Functional Magnetic Resonance Imaging
 - Uses changes in blood oxygen levels to detect areas of brain activity
 - Is effective, but expensive to implement

Pulse Echo Ultrasound

- Transmits and receives ultrasonic pulses through a transducer
- Is effective and less expensive, but requires complex hardware

Pulse Echo Ultrasound

A pulse signal, or excitation signal, is transmitted through the transducer

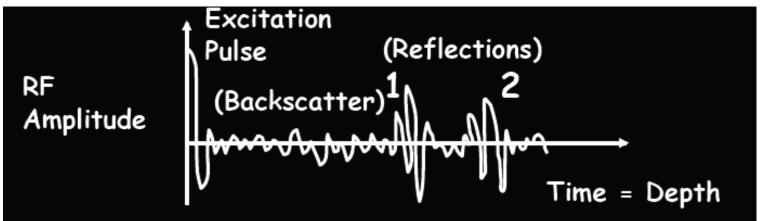
The acoustic signal is reflected back to the probe once it reaches boundaries between tissues

The amount of delay between transmitting a pulse and receiving a pulse indicates the depth of tissue

Pulse Echo Ultrasound

Illustration of Pulse Echo Ultrasound TX and RX

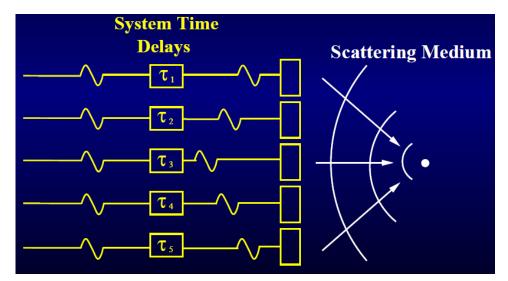
Reflected signals can be used to form an image based upon their time delay



[REF] Yao Wang, "Medical Imaging", 2009, http://eeweb.poly.edu/~yao/EL5823/MI_Ultrasound2_2012_turnbull.pdf

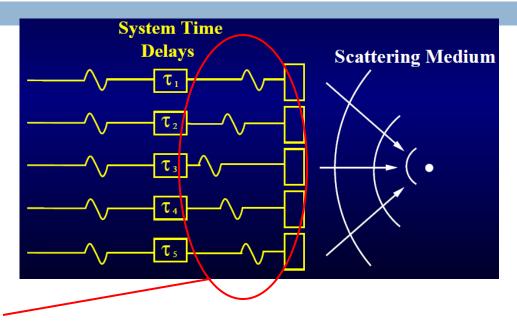
Problem Statement

- Produce a low-cost Pulse Echo Ultrasound System
- System sends and receives pulses through 128 elements of a transducer
 - Phase and amplitude are controlled
- Recovered signals can be processed to form an image



[REF] Mark L. Palmeri, "Ultrasound Beamforming and Image Formation, 2007

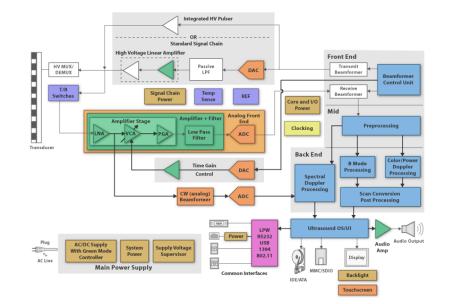
Problem Statement



- Different delays allow for the transducer to focus energy on a specific point
 - Allows for more power to be transmitted to a specific region of interest, more power is reflected back that can be processed



- Researched approaches used by industry and used design resources and ASICS created by semiconductor companies (Texas Instruments, Maxim)
- Utilized contacts professors in the department had to obtain some components for the system

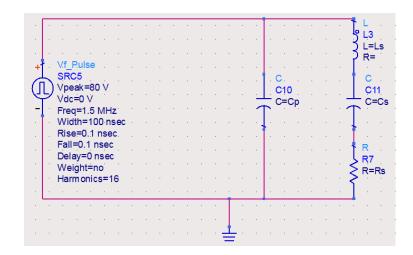


Design – Functional Requirements

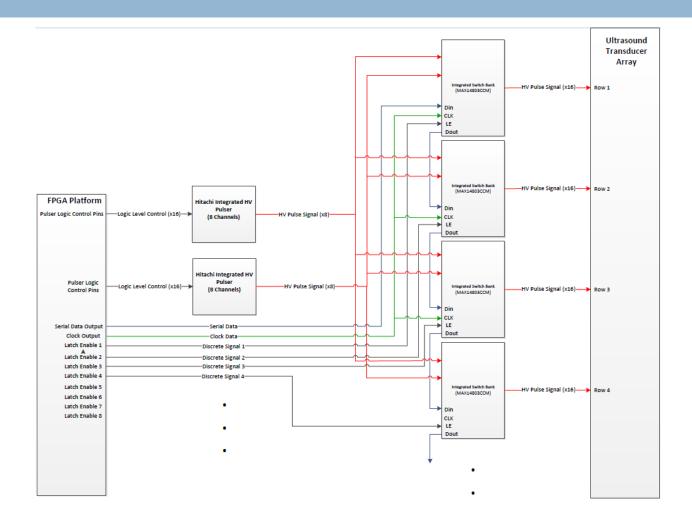
- Waveform Generator must be controlled by a simple user interface provided by an FPGA development board
- Generated pulse delay must be controllable from 10ns to 20 us
- Pulse amplitude must be controllable from OV to 80V
- Individually control a linear array of 128 elements
- Recover reflected pulses through receiver circuitry

Meeting Technical Requirements

- Phase Control: Utilize a 200 MHz oscillator to drive counter circuits for each channel
- Amplitude Control: Utilize the impedance of the transducer to filter a PWM signal

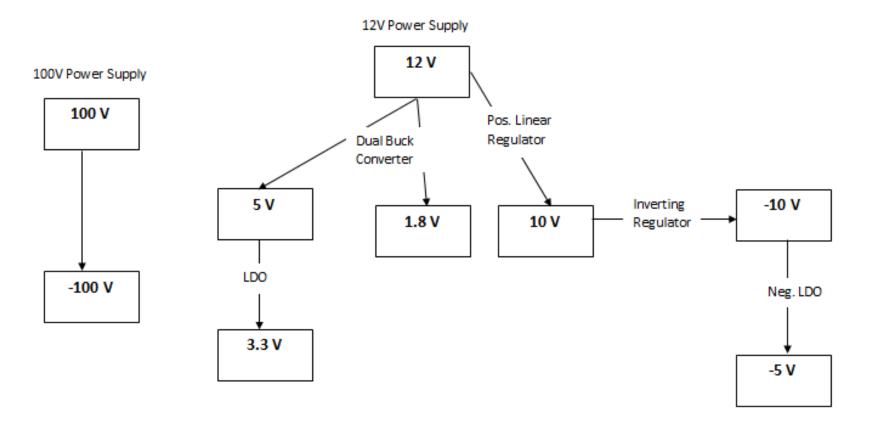


Design – Block Diagram



Power Electronics

Power Regulation



Dual Buck Converter Design

$$\mathsf{D}_{\mathsf{min}} \approx \frac{\mathsf{V}_{\mathsf{OUT}} + \mathsf{V}_{\mathsf{FD}}}{\mathsf{V}_{\mathsf{IN}(\mathsf{max})} + \mathsf{V}_{\mathsf{FD}}}$$

$$D_{5V,min} = \frac{5V + 0.5V}{12V + 0.5V} = 44\%$$

$$L_{min} \approx \frac{V_{IN(max)} - V_{OUT}}{I_{LRIP(max)}} \times D_{min} \times \frac{1}{f_{SW}}$$

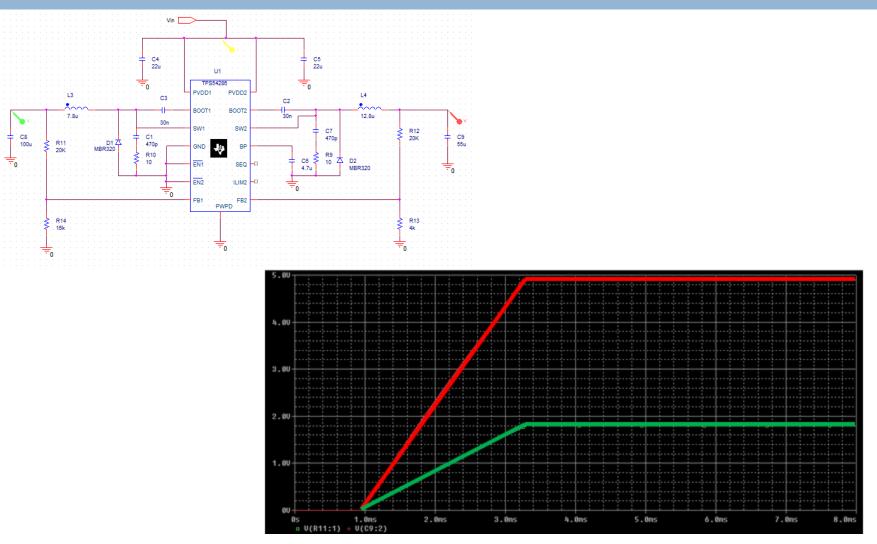
$$L_{5V,min} = \frac{12V - 5V}{600mA} \times 44\% \times \frac{1}{600kHz} = 12.8\mu H$$

$$C_{OUT} = \frac{1}{4 \times \pi^2 \times (f_{RES})^2 \times L}$$

$$C_{5V,OUT} = \frac{1}{4 \times \pi^2 \times 6000 Hz^2 \times 12.8 \mu H} = 55 \mu F$$

$$R13 = \frac{V_{FB} \times R12}{V_{OUT1} - V_{FB}}$$

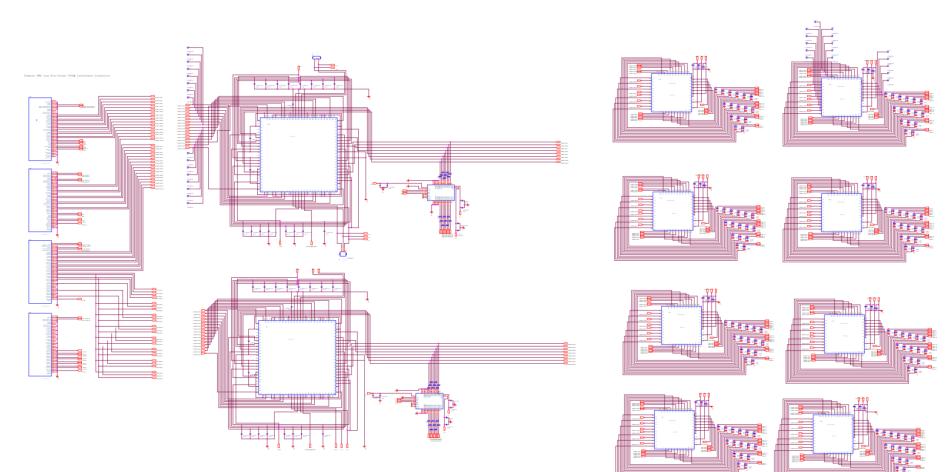
Dual Buck Converter



Group: Dec1204

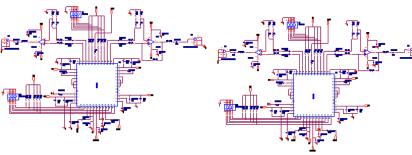
Schematics – Pulse Echo Ultrasound

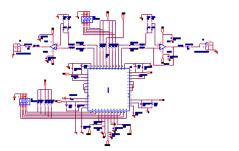
Transmit

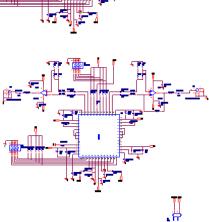


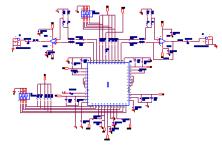
Schematics – Pulse Echo Ultrasound

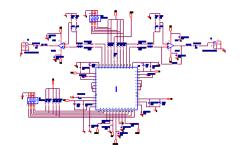
□ Receive

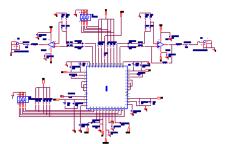


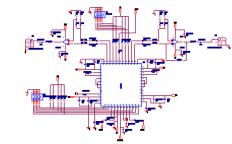




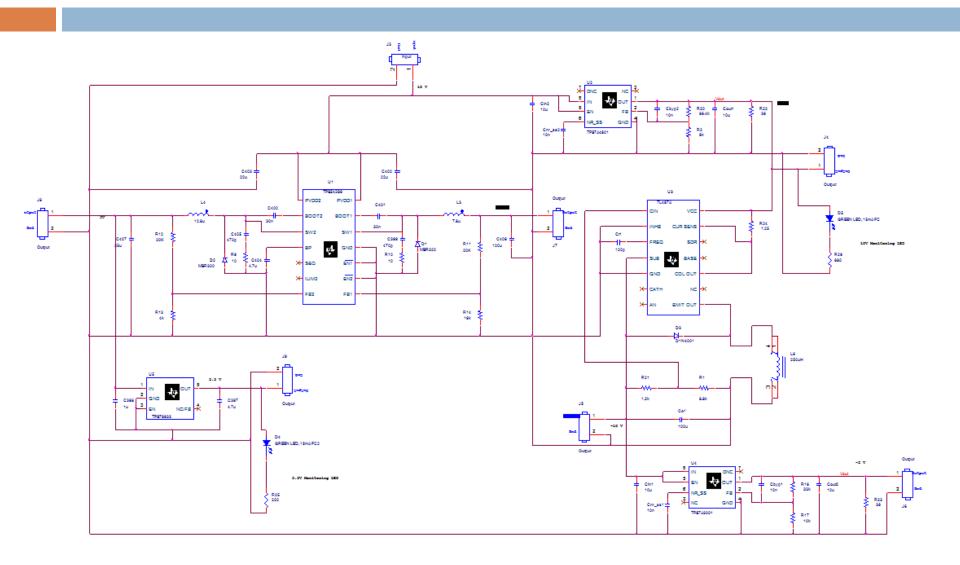








Schematics – Power Electronics



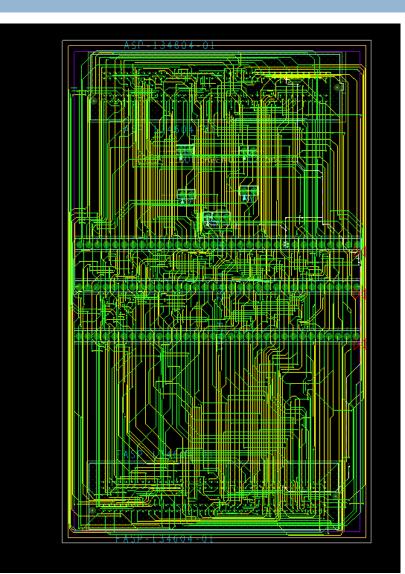
FPGA Results

				2,275.563 ns	5					
Name	Value		2,200 r	s Lluuu	2,400 ns	2,600 ns	2,800 ns	3,000 ns	3,200 ns	3,400 ns
្ន្រី serial_clk	0									
🔓 pulser_clk	1									
ustart_seq	1									
□ o_serial_clk	0									
Image: pulser1_ctl[15:0]	0101010101010110	10101010101010	10	010101	0101010101	101010101010	01010	010101010101010101	0000000	0000000
Image: Second State S	1010101010101010	101010101010	1010	010	101010101010101	10101010	10101010	01010101010101	000000	00000000
🖓 serial_data	0									
🌆 clear_output	0								ALC PLOTS MEN	
▶ 📑 le_out[7:0]	11111111					111111	11			
🗓 begin_program	1									
Iatch_select[2:0	000					000				001
🗓 serial_done	1									
# pulser_done[15	000000000000000000000000000000000000000				000000	000000000			111111	11111111
🕨 🌃 pulser_1_phase	[1,10,11,100,101,1					[1,10,11,100,101,1	10,111,1000]			
🕨 🌃 pulser_2_phase	[1001,1010,1011,11				[1001,	1010,1011,1100,110	1,1110,1111,10000	1		
🕼 count	0					0			X	1
▶ 式 v_lvl[0:1]	11					11				
		X1: 2,275.563 n:						Ni		

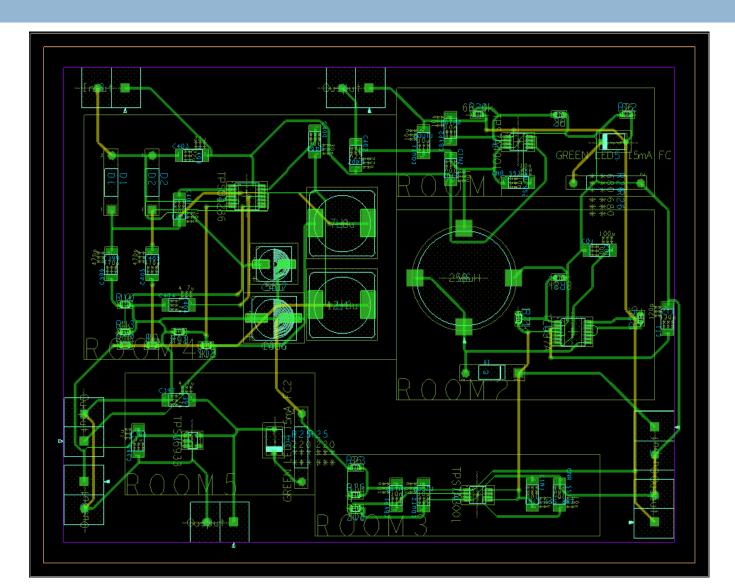
Designed a state machine to control transmitter hardware with strict timing requirements

PCB Layout – Pulse Echo Ultrasound

PCB Layout – Connector Board



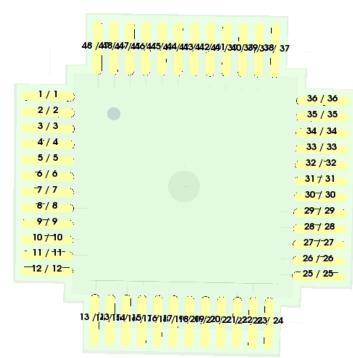
PCB Layout – Power Electronics



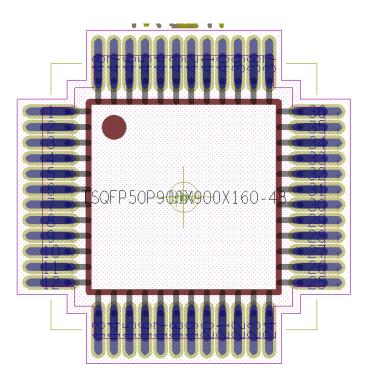
PCB – Footprints & Padstacks

Switch Bank MAX140803CCM

Footprint



Padstack

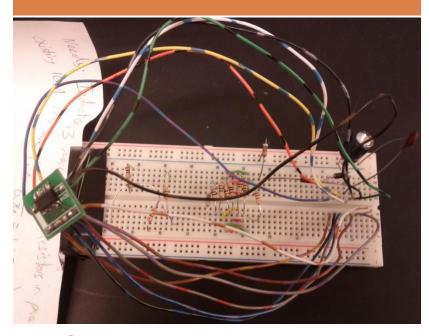




- Integrated circuits were originally tested in PSPICE if the models were available
- Most devices do not have PSPICE models
- Tested the physical ICs on a breadboard based off the PSPICE schematics
- Provided verification of schematics

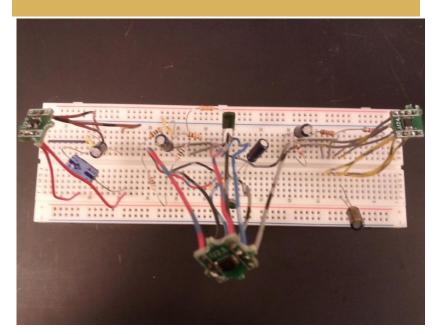
Testing - Power Electronics

Inverting Regulator



Could not test due to a lack of a breadboard inductor

Linear Regulators



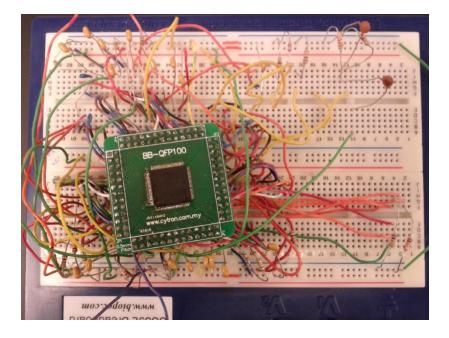
Positive, Negative, and
 3.3 linear regulators
 performed to spec

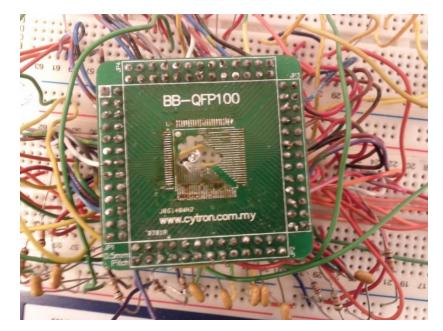
Testing - Pulser

Breadboard Pulser IC

Testing the proper circuit setup to run the IC

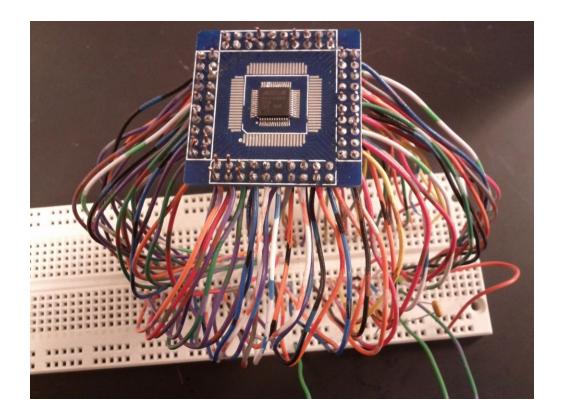
Unable to test further due to destruction of wafer





Testing - Switch Bank

- Breadboard Switch Bank IC
 - Tested to see if channels can be opened and closed



Challenges

- Working backwards
- Limited FPGA Experience
- Limited PCB Layout Experience
- Bread boarding and testing of ICs
 - Pulser
 - Switch Bank
 - Power Electronics

Recent Changes

- □ Final PCB Product was too expensive
 - Cost for 6-layer board is ~\$1000
- Designed a 16-channel version of our final product
 Estimated cost ~\$500
- Acquired additional funding November 28th
 - Went back to original design

Cost Estimates – Testing and Final Product

Part:	Part Description:	Cost:
ML605 Evaluation Kit	XLINX FPGA Board	\$1,800
FMC XM101 LVDS QSE Mezzanine Card	FPGA breakout board for LVDS pins with QSE Connectors	\$700
AFE5808EVM	Analog Front End Analog to Digital Converter Evaluation Board	\$299 x 6= \$1,794.00
TSW1250EVM	Analysis system	\$650.00
TX810	Transmit/Receive Switch	\$11.16 x 10 = \$111.60
HDL6V5581	HV Pulser	\$0
MAX14803CCM	High-Voltage Switch Bank	\$26.91 x 14 = \$376.74
Ultrasound Probe		\$15,000.00
Power Electronics	Regulators and Converters	\$320.19
Resistors, Capacitors, Inductors		\$173.86
Connectors	Transducer and Mezzanine card connectors	\$264.03
PCB Fabrication		\$1000
Total Cost		\$22,190.42

Group: Dec1204

Remaining Work

- □ Final PCB product is currently being fabricated
- Solutions developed will continue to be used
- Focus on leaving documentation for future work
- Future development of design
 - Direct control of 512 ultrasound elements

Questions?