Design Document

For a Pulse Echo Ultrasound System

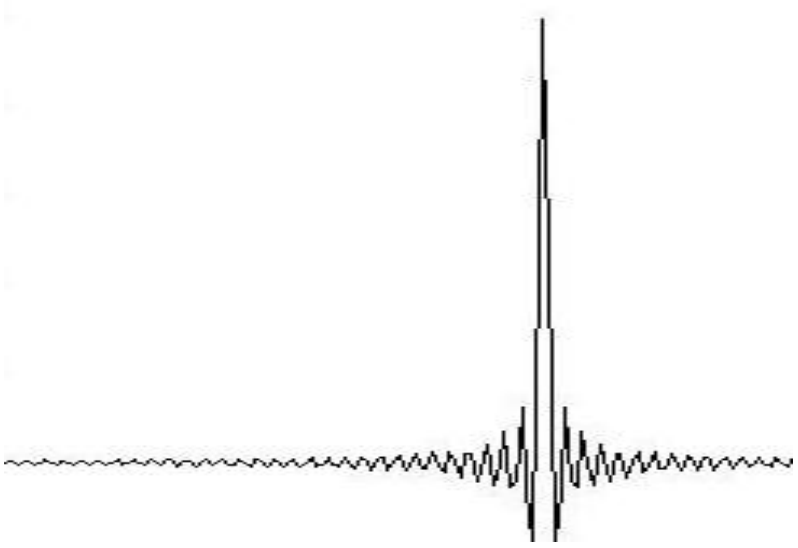

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Table of Commonly Used Terms

Term	Meaning
"Pulser"	A device that can provide square wave pulses
"High Voltage" or "HV"	A voltage level ranging form 20V to 100V
"Analog Front End"	A device made by Texas Instruments that incorporates all the necessary hardware to recover ultrasound signals into one package.
"Multiplexing"	Switching a small number of inputs amongst a larger number of outputs

Problem Statement

In order to understand the project, a brief description of brain-imaging technology will be given. One technology that will be evaluated is fMRI. Functional magnetic resonance imaging (fMRI) is a noninvasive test that uses a strong magnetic field and radio waves to look at blood flow in the brain and detect areas of activity. Oxygen-rich blood and oxygen-poor blood have a different magnetic resonance. The most active areas of our brain receive more oxygenated blood. The advantage in fMRI is that it does not emit radiation like X-rays, computed tomography, and positron emission tomography scans. Although the fMRI is a very effective brain-imaging system, it is also very expensive. In Lieu of such high costs, the design of a pulse echo ultrasound system was pursued. A pulse echo system consists of a transducer assembled with 128 small individual elements that can each be pulsed separately. The purpose of pulsing each element separately is to allow for a phased-array of signals (signals with different phases ranging from 10ns to 20us) to be sent through the ultrasound probe. Additionally, pulse echo ultrasound millions of pulses and echoes are sent and received each second. These sound waves are reflected back to the probe once a boundary between tissues is found, and the reflected signals can be processed to form an ultrasound image.

An ultrasound circuit is composed of many parts that serve different functions. The design that is being used has eight major components that define the circuit. The components are as follows: waveform generator, high voltage amplifiers, transmit/receive circuit, ultrasound transducer, low-noise amplifiers, and variable-gain amplifiers. A block diagram of the system is shown below in Figure 1 where you can see the relations of the components.

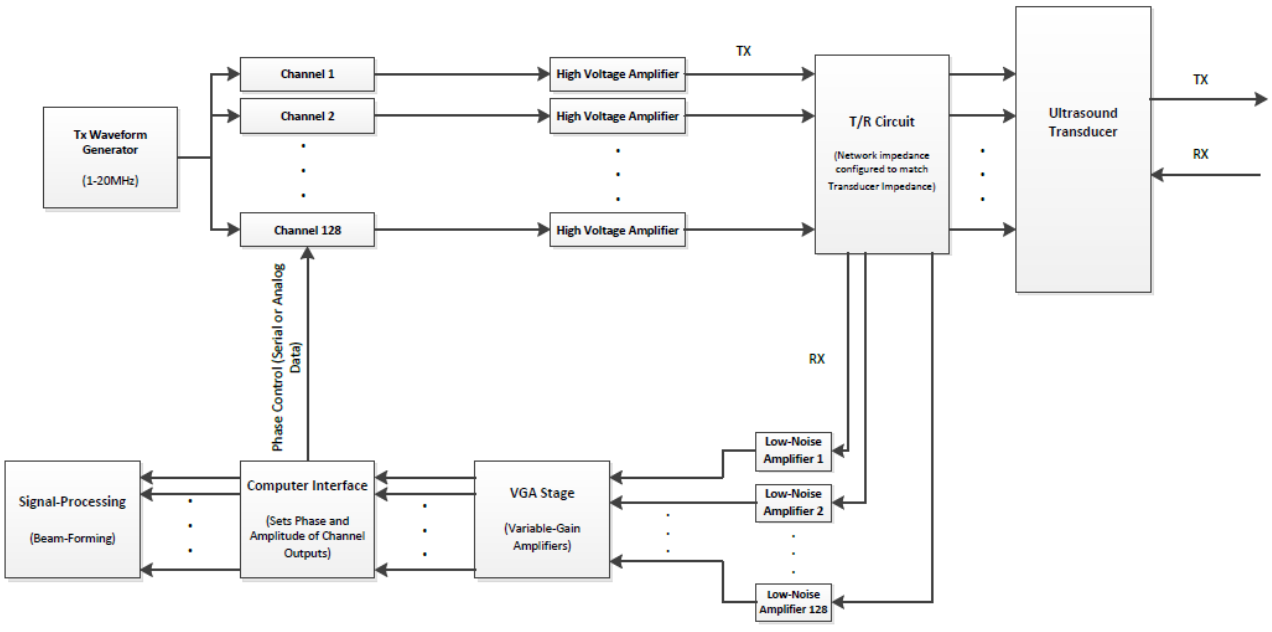

Figure 1 - Block Diagram of the Ultrasound System

A brief description of each system component shown in the block diagram is given below.

Waveform Generator

The waveform generator generates digital samples of 3 MHz ultrasound pulses. A high-speed DAC will be used to convert the digital waveforms to the analog domain. In total, 128 individual signals will be generated by this functional block.

High Voltage Amplifier

High voltage amplification of the generated pulses is necessary in order to provide enough energy to the ultrasound transducer (due to poor electrical to acoustic energy conversion within the transducer). A stronger signal means that there is less opportunity for signal loss while being transmitted. The maximum voltage that this component will generate is 100 VDC, or 200V peak-peak.

Transmit/Receive Circuit

The transmit/receive circuit will transmit the amplified pulses to the ultrasound transducer. It will receive the reflected low voltage signals from the transducer and use them for the signal processing of the ultrasound. The transmit/receive circuit will also prevent high-voltage pulses from entering the receiver circuitry.

Low-Noise Amplifier

The low-noise amplifier will amplify the weak reflected signals that the transmit/receive circuit receives from the ultrasound transducer. It's placement after the receiver is to recover the low-power reflected ultrasonic signal in the presence of significant noise.

Variable-Gain Amplifier

A variable-gain amplifier is placed after the low-noise amplifier and is used to map the signal into the appropriate dynamic range for signal processing. Computerized control of this device will allow for the gain to be adjusted appropriately over time.

Computer Interface

A computer interface will be used to control the phase and magnitude of the waveform generator channel outputs. The delay range is 10 ns – 20 us. Additionally, recovered signals will be sent to the computer interface for signal processing and recovery.

Signal Processing

Recovered (reflected) ultrasound pulses will be amplified and communicated to the computer interface for digital signal processing and imaging. All signal processing will be done in the computer interface.

Transducer

The transducer, otherwise known as the probe, is the component in the system that has contact with the body. The basic function of the transducer is to receive an electrical pulse and convert it into a acoustic vibration at a pre-determined frequency. Ultrasonic pulses reflected off of the body are captured by the transducer and converted into electrical signals that can be processed to form images.

Resource requirements

The technical requirements, system requirements, and user interface requirements are given in the tables below. Highlighted text indicates that the information is unknown at this point.

Table 1 - Resource Requirement Descriptions

System Component:	Requirement Description:

Waveform Generator	The waveform generator shall be capable of controlling the pulser integrated circuits in order to produce high-voltage signals. Each output must be individually controllable in order to implement a phased-array system.
Waveform Generator	The waveform generator shall be capable of being controlled by the user interface.
High Voltage Amplifier (Pulser)	The high voltage amplifier shall be capable of amplifying the input waveform so the output has a pulse amplitude 190 Vpp.
High Voltage Amplifier (Pulser)	The amplifier circuit shall have a bandwidth that exceeds 3 MHz.
T/R Circuit	The T/R circuit shall function as protection against high-voltage transients for the receiver. However, the T/R circuit shall allow high-voltage transmitted signals to propagate to the Ultrasound Transducer.
T/R Circuit	The T/R circuit shall only allow a signal with maximum amplitude of X V to enter the receiver circuit.
T/R Circuit	The T/R circuit shall have impedance matching with the Ultrasound Transducer. (Note: Ultrasound Transducer Electrical Characteristics are unknown at this point)
Analog Front End	The Analog Front End shall contain a low-noise amplifier to recover a small-magnitude signal from the transducer output.
Analog Front End	The Analog Front End shall contain a variable gain amplifier with an adjustable gain.
Analog Front End	The Analog Front End shall contain an ADC capable of sampling at 50MSPS and that produces serial LVDS data at the output.
Transducer	Operates in the 3 MHz frequency range
Transducer	Linear array with 128 elements

System Analysis

Ultrasound technology has rapidly evolved in the past few decades. Several large companies such as Texas Instruments and Maxim have extensive portfolios of ultrasound-specific integrated circuit products. Our team elected to primarily use Texas Instrument products, due to the fact that Texas Instruments is willing to donate products and services to senior design teams.

In order to select the different components we need for our system, we followed the suggestions of the following flow-chart provided on Texas Instruments' website:

[REF] http://www.ti.com/solution/ultrasound_system

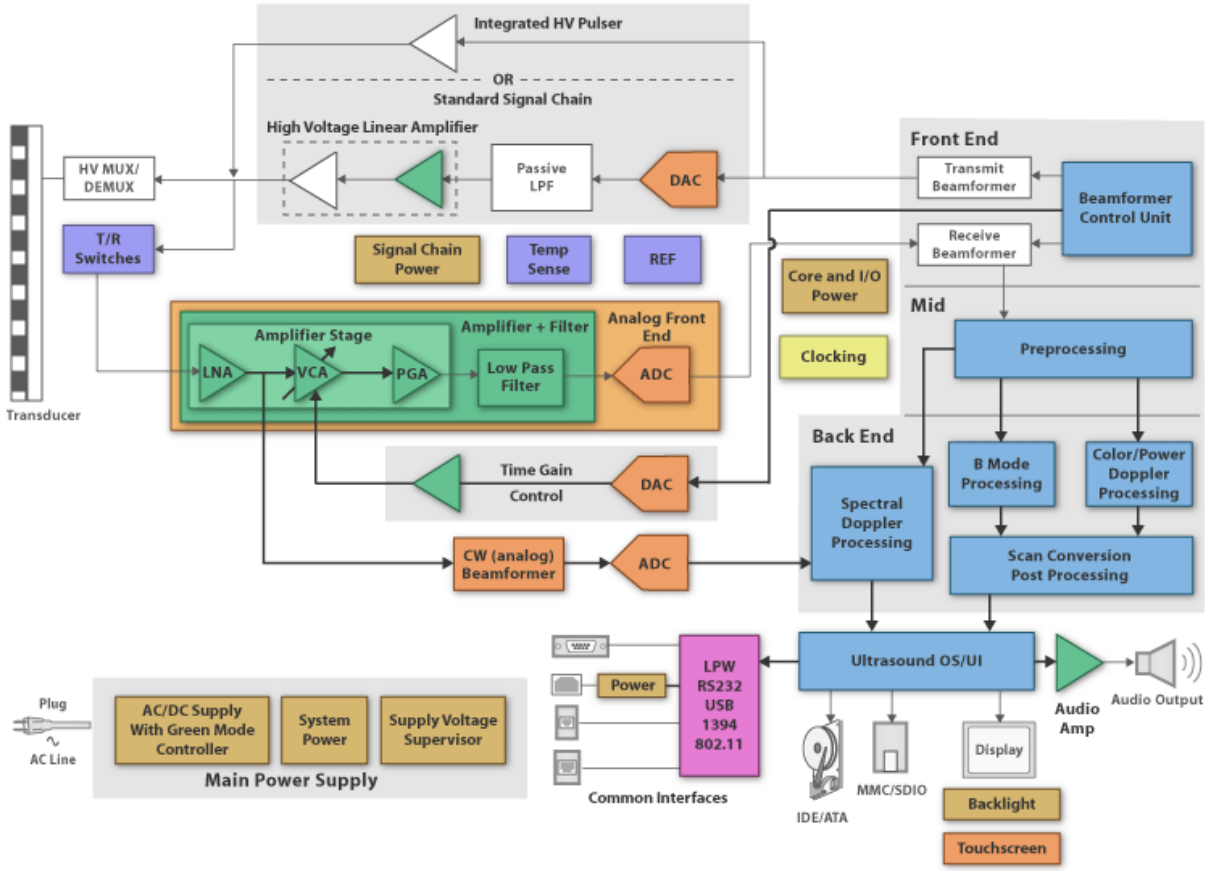

Figure 1 - Block Diagram with Suggested Texas Instruments Products

Using this flow-chart, we selected the following products to use for our design:

- TX810 – Integrated T/R Switch
- AFE5808 – Analog Front-End Integrated Circuit
- Texas Instruments Voltage Regulators

Out of all the components listed above, the most consideration was placed into the component to be used for digital waveform generation and acquisition. At first, our team assumed that ADC and DAC cards with 32-128 I/O pins would be readily available in the market with the specifications we desired. However, after contacting several vendors, it was determined that there is no cost-effective solution to implementing these

functions with existing products. Therefore, we have decided to use a XLINX FPGA development board to perform signal generation and transmitter control operations.

Details for each component and its electrical characteristics are given in the "Detailed Design" portion of this document. Comments regarding functionality and design trade-offs for each component are also given in the "Detailed Design" portion of this document.

Detailed Design - Transmitter

The detailed design information for the ultrasound system is given in this section. The entire design is broken down into individual functional parts in order to increase readability and understanding. A detailed block diagram of the transmit circuit is included in Figure 5 in order to give better insight into the entire design, and should be referenced to clarify confusion regarding system architecture. This diagram gives a description of interfaces between the following functional blocks:

- Waveform Generation (FPGA Platform)
- High Voltage Pulser
- Output Multiplexing (Integrated Switch Banks)

Each of the functional blocks listed (Waveform Generation, High Voltage Pulser, and Output Multiplexing) is described below in greater detail. Descriptions of the devices and components selected to perform each function are also given. Once all of the functional blocks have been described, the overall transmit block diagram in Figure 5 is introduced to give insight into the architecture of the entire system.

Waveform Generation

The waveform generation for the ultrasound system will be accomplished by using an XLINX ML605 FGPA development board. Specifically, this FPGA board will provide logic control for the pulser integrated circuits (described in the next section). The FGPA board will also control the interface between the circuitry and the ultrasound transducer, which is described in the section "Output Multiplexing". The table below describes the important specifications of the FPGA board and relates them to the system requirements for the waveform generation functional block.

Parameter	Device Specification	Required Specification
Output Signaling Speed	Up to 7GHz	50-100MHz
Programmability and Debugging Interface	Easily programmable through a ISE Design Suite	Programmable through a computer interface
Outputs	2 FMC Connectors: The first is a high pin count (HPC) configuration that provides connectivity for 160 single-ended or 80 differential user-defined signals. The second is a low pin count (LPC) configuration that provides connectivity for 68 single-ended or 34 differential signals.	64 I/O pins that can be used to control the pulser logic inputs.

Expandable Memory Option	Included	Desired

The table illustrates that the FGOA board is appropriate for our purposes.
The XLINX ML605 FPGA evaluation board is shown below in Figure 2.

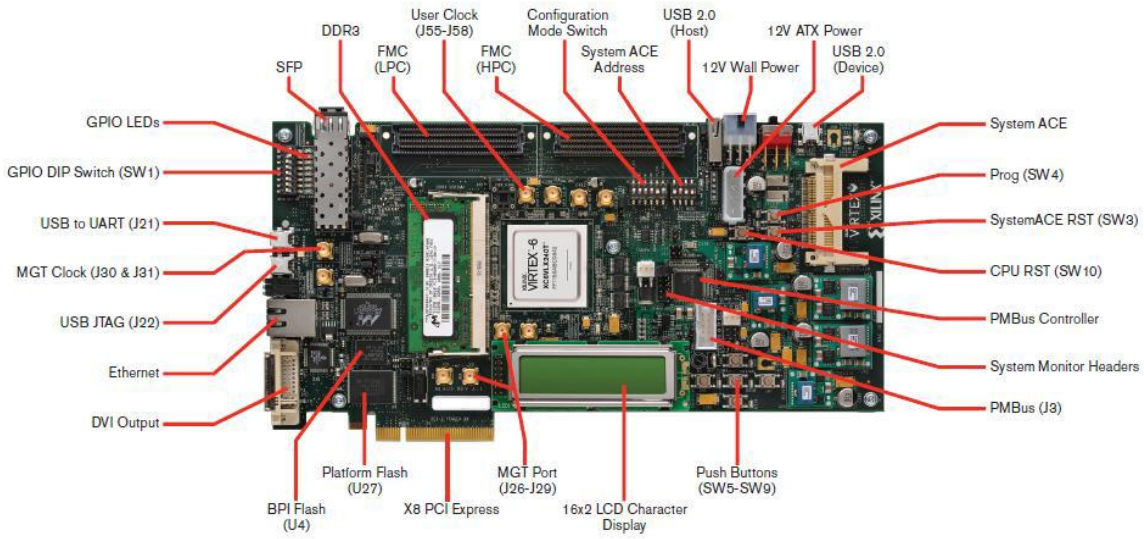

Figure 2 - Image of FPGA Evaluation Board

Once the evaluation board shown in Figure 2 is received, the following items will be thoroughly tested:

- Output signaling interface to pulser inputs
- programmability
- confirm the number of available outputs

Once the functionality of the device is confirmed, the device will be used to drive a 32-channel ultrasound system transmitter circuit.

High Voltage Pulser

High voltage switching will be accomplished by using an integrated circuit designed specifically for the task. Hitachi semiconductor has an extensive line of ultrasound-specific integrated circuits, and we will utilize the HDL6V5581. The essential specifications for the device are listed in the table below.

Parameter	Device Specification	Required Specification
Bipolar output voltage limits	+/- 105V	+/-100V
Frequency Range of Operation	1 MHz – 25 MHz	3 MHz
Number of Channels	8	4-32 channels desired
Switching Delay Time	24ns	Less than 167ns

The HDL6V5581 will be utilized using the circuit shown below (note: only input and output pin interfaces are detailed in Figure 3:

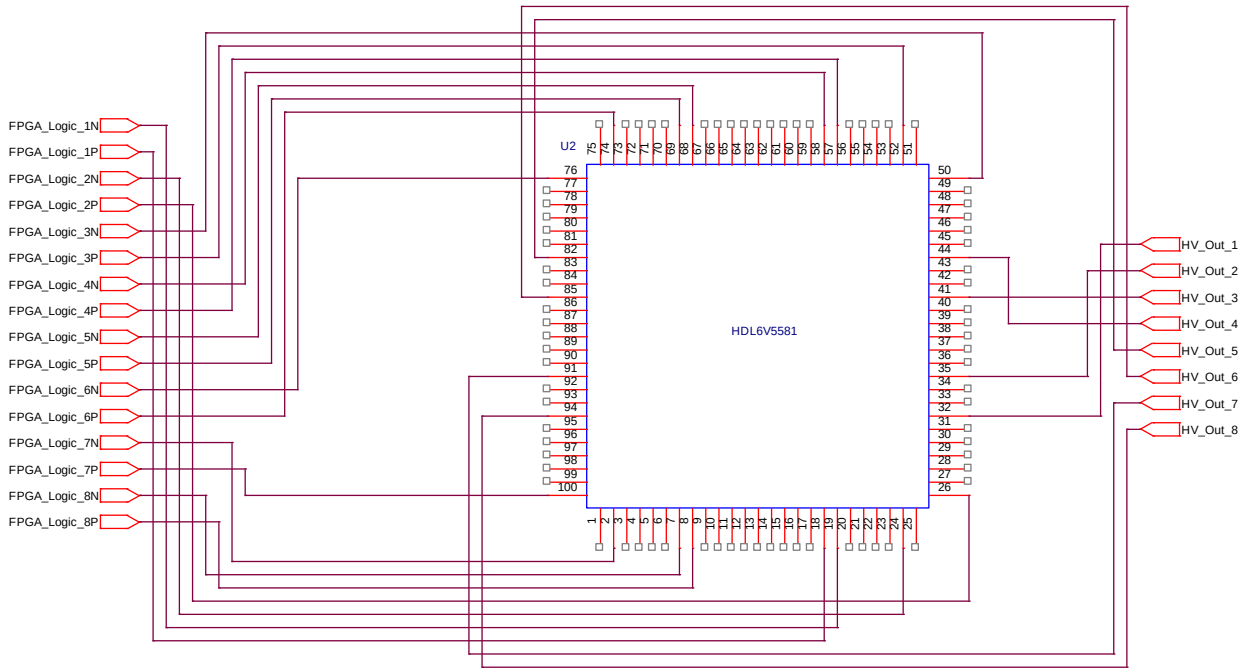

Figure 3 – HDL6V5581 Application Circuit

The application circuit follows the suggestions given in the HDL6V5581 datasheet. It should also be noted that the power interfaces of the device are not detailed in Figure 3. The power pins will follow the suggestions given in the HDL6V5581 datasheet regarding bypass capacitor placement and board layout.

The inputs to the HDL6V5581 will be provided by the XLINX FPGA evaluation board. A table illustrating the input pins and interface with other devices is given below:

Input Pin Name:	Logical Characteristics:	Incoming Signal from:
Pin#	If this pin receives a "high" signal, the output is pulled down to the VPP_ voltage	FGPA HPC connector
Nin#	If this pin receives a "high" signal, then the output is pulled up to the VNN_ voltage	FPGA HPC connector
EN	Enables all of the channels if driven low	Will be enabled by the computer interface

Note: The inputs to the HDL6V5581 will be logical CMOS signals ranging from 0 to 5V. The XLINX FPGA board is capable of signaling speeds of up to 7 GHZ, which will be adequate for producing small duty-cycle (~10%) 3 MHz signals.

Next, a brief description of the operation of the HDL6V5581 will be given in order to understand how the device will operate. The HDL6V5581 will drive two different power MOSFETS in order to perform high

voltage switching. The equivalent circuit for one channel of the device is shown below in Figure 4.

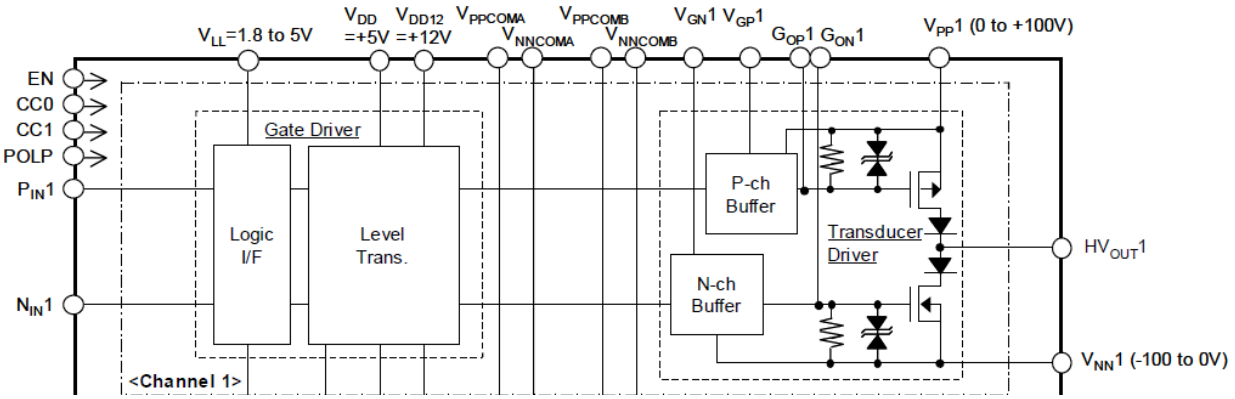

Figure 4 - Equivalent Circuit for High Voltage Switching

In Figure 4, the MOSFET gates are driven by specialized circuitry in order to "turn on" the devices. The gate-driver circuitry is labeled as "Level Trans." in the Figure above. When "high" logical signals are applied to the Ninx pins, the N-Channel MOSFET will current from the 100V source and pull the output voltage to 100V. When "high" logical signals are applied to the Pinx pins, the P-channel MOSFET will conduct and pull the output voltage down to -100V. Essentially, the HDL6V5581 allows for two individual logic control signals to control power MOSFETs that switch high voltages into the signal path.

The outputs of the application circuit shown in Figure 3 are +/-100V amplitude pulses that will be sent to the ultrasonic transducer. Each output of the pulser circuit can source/sink up to 2.5A, which indicates that the entire ultrasound transmitter will draw up to 80A during a transmission. The interface between the pulser and the ultrasound probe will be described in more detail later in this report.

Output Multiplexing

In order to reduce the amount of hardware needed to drive a 128-element transducer, the outputs of the transmitter can be multiplexed to the ultrasound interface. Such multiplexing allows for a small amount of circuit outputs to connect to the large number of ultrasound elements. Utilizing this concept, this ultrasound system design will only consist of a 32-channel transmitter/receiver circuit that will be switched to connect to all of the 128 transducer elements. Figure 5 illustrates this concept in relation to the other hardware that has been introduced in this document.

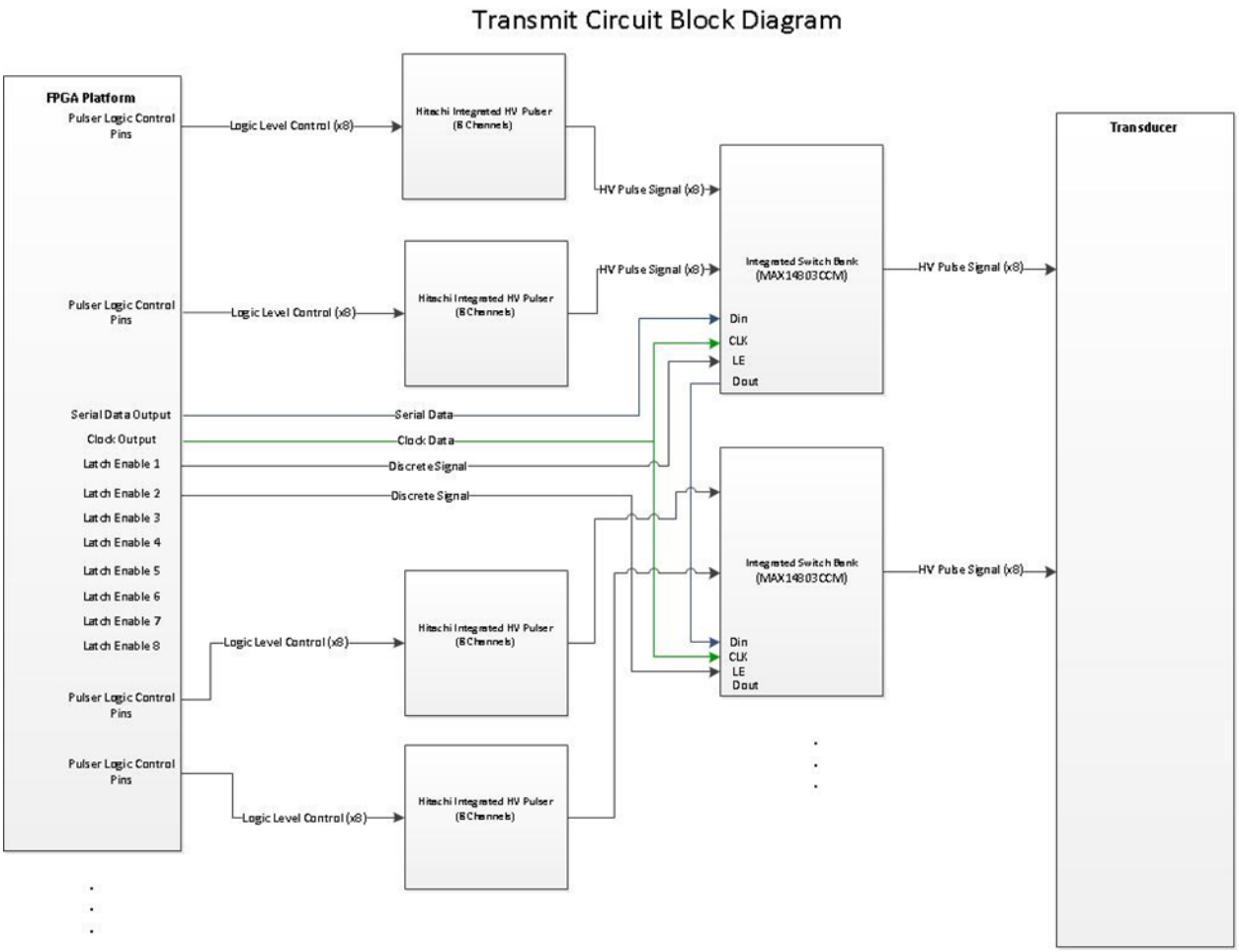

Figure 5 – Ultrasound Output Multiplexing

While Figure 5 details numerous interfaces between devices, the general operation of the circuit can be understood by examining it carefully. The FPGA control of the Hitachi Pulsers, which was explained thoroughly proceeding this section, is shown at the left-most side of the diagram. Moving right in Figure 5, the outputs of the Hitachi pulser are shown to be connected to "Integrated Switch Bank" blocks. Each of the "Integrated Switch Bank" blocks consists of 16 serial-programmable SPST switches that connect directly to the ultrasound transducer elements. Therefore, it is possible to connect four eight-output Hitachi pulsers (32 outputs total) to an array of eight 16-channel Integrated switch banks (128 outputs total) that connect to 128 ultrasound transducer elements. The outputs of the pulsers can then simply be multiplexed to the ultrasound transducer in any order by enabling which switches are "on" via a serial interface.

Another aspect of Figure 5 to note is that only one serial interface is used to program all of the Integrated Switch Banks. The MAX14803 Integrated Switch Bank has both a serial input and serial data output, and the serial data output can be sent to another device input. Therefore, the serial interfaces for the devices can be daisy-chained together to allow for one interface to program all of the switch banks. In order to control which device(s) are being programmed, "Latch Enable" pins are present on each device that control whether to hold a previous set of values or load new values.

Specifications for the MAX 14803 Integrated Switch Bank are listed below:

Parameter:	MAX14803 Specifications:	Desired Value:
Number of Available Switches	16 integrated SPST switches	Desired: An integrated array of 16-32 switches
Maximum Voltage/Current Limits	Up to +100V/-100V Voltage on each channel. Up to 3A of current on each channel	Handles up to +100V/-100V Handles up to 2.5A of current per channel.
Serial Interface	Each device features a 20MHz serial interface that operates at 5V. Serial interfaces between devices can be daisy-chained for simplified control. "Latch Enable" pins control whether the devices retains its currently programmed state or loads a new state in.	The device will feature an interface that will allow for each switch to be controlled individually.

From the table above, it is evident that the Integrated Switch Bank will be a suitable component for the design.

Detailed Design - Receiver

Only the transmitter circuit and functionality has been described up to this point in the Detailed Design section. However, with pulse-echo ultrasound, the objective is to acquire reflected pulse signals in order to obtain a good view of the brain. An outline of the receiver design in shown below in Figure 6.

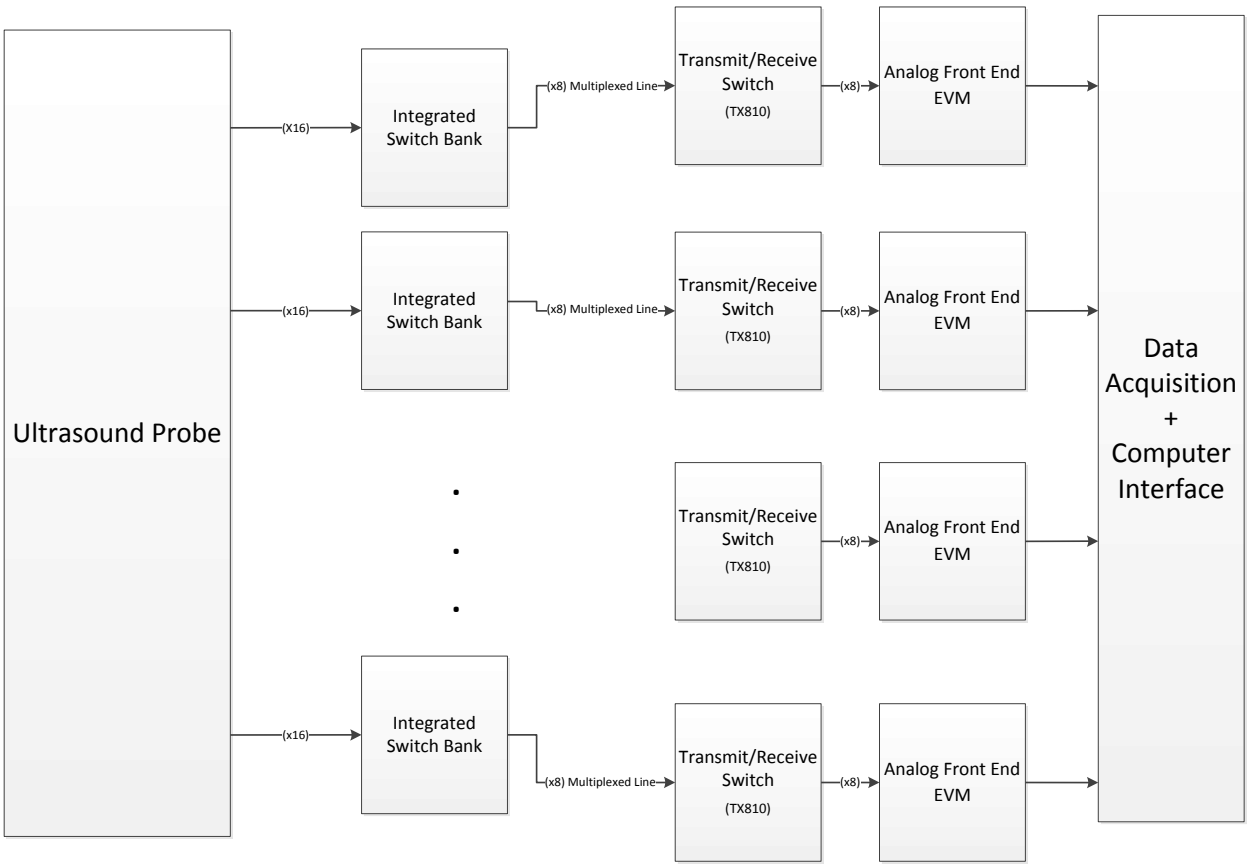

Figure 6 - Ultrasound Receiver Block Diagram

Figure 6 details multiple interfaces between components, and the objective of the next section is to explain the functionality of each component and its interface to other devices.

Integrated Switch Bank

This component was discussed thoroughly in the previous section that described the transmitter operation. Please refer to this section for details.

Transmit/Receive Switch

Ultrasound pulses must be both sent and received through the same channels of the transducer in order for the system to function. Therefore, a method of protecting the receiver from the high-voltage signals being sent by the transmitter must be devised. Fortunately, Texas Instruments has developed an integrated circuit (the TX810) that incorporates diode bridges for eight channels into a single package. The equivalent circuit for this device is shown in Figure 7.

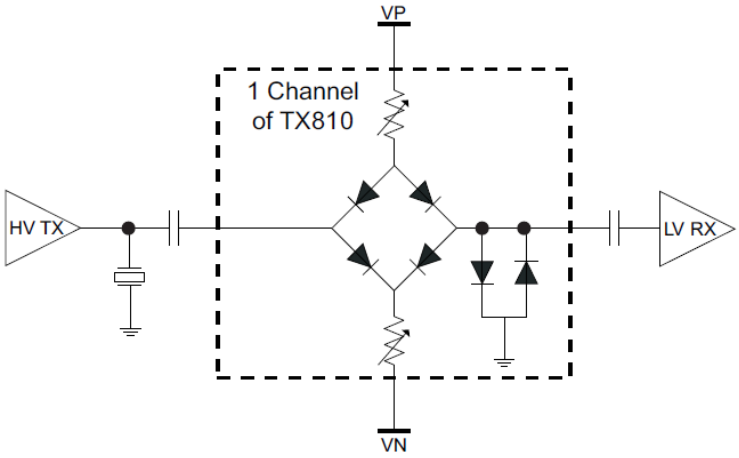

Figure 7 - Equivalent Circuit of the TX810 Transmit/Receive Switch

By observing the circuit in Figure 7, it can be seen that signals with a magnitude greater than VP and VN will not be passed to the "LV RX" pins. Therefore, this device will only allow small-amplitude signals to pass to the receiver.

Analog Front End

The Analog Front End is an integrated circuit, manufactured by Texas Instruments, that incorporates all of the functions needed to recover an ultrasonic pulse into a single package. An equivalent circuit of the device is shown below.

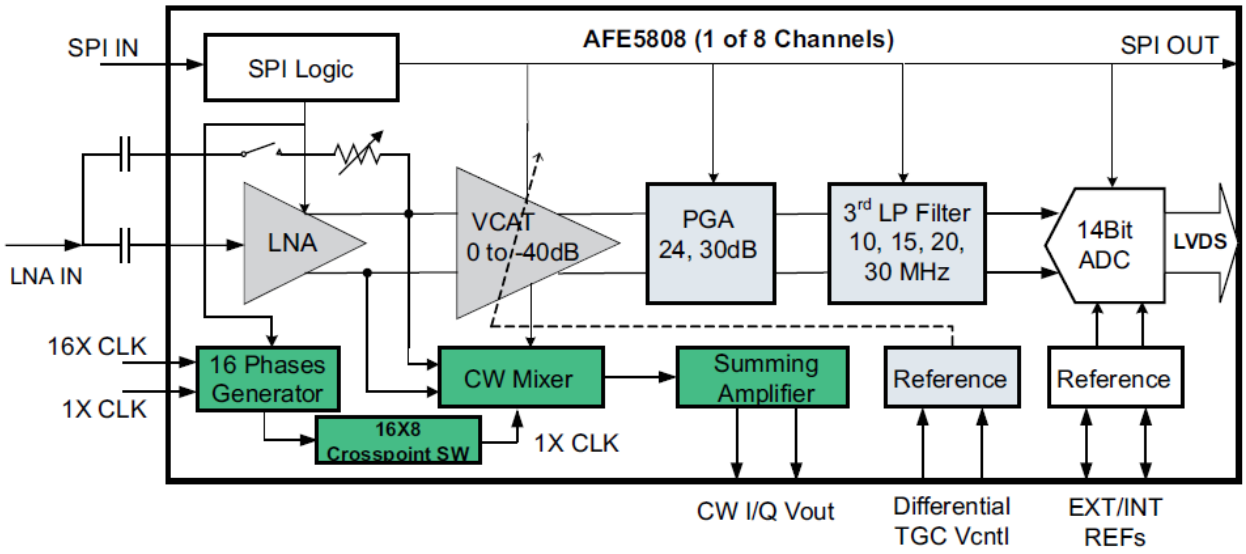

Figure 8 - Equivalent Circuit of One Channel of The AFE5808

While the device itself incorporates a significant amount of functionality into one package, our team has elected to purchase a set of evaluation boards that contain the device. These evaluation boards have all of the interfaces to the AFE5808 broken out so it can be easily incorporated into the existing ultrasound system design.

With using the AFE5808EVM as the analog front end on its own, the team will able to also use the test features of the board. The main features of this are

- Continuous wave test
- 8 channel low-voltage differential signal (LVDS) outputs from the ADC

Along with using the test features built into the AFE5808, we will be using the TSW1250EVM to further test and analyze the AFE5808. The AFE5808 and TSW1250EVM are pictured below in Figure 9.

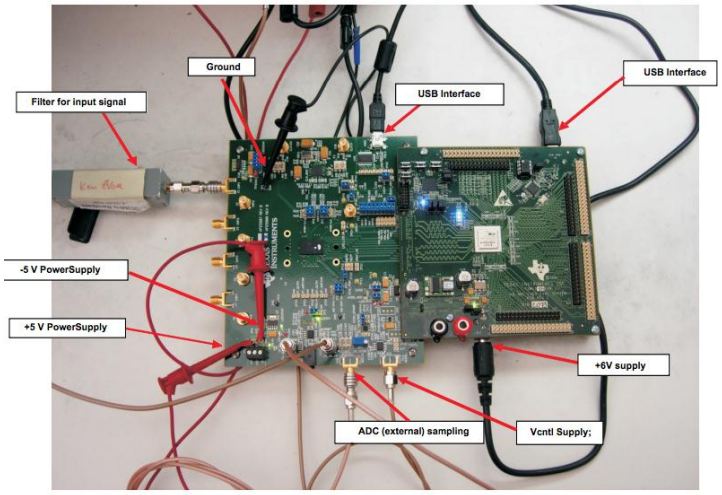

Figure 9 - Image of a Test Set-up for the Analog Front End Evaluation Module

The TSW1250EVM connects directly into the AFE5808 and can analyze the AFE5808's LVDS data stream. The TSW1250EVM interfaces to a computer, much like the AFE5808, through USB and has GUI software that is provided with the board. The main features of the board are

- High-speed ADC with LVDS output
- 64k capture depth with USB transfer

The evaluation boards and GUI provide an effective way to demonstrate that the AFE5808 is performing at expected data sheet specifications.

Detailed Design – Power Electronics

Two separate power sources will be used to power the system's device circuitry. The main power supply will be 12V; while there will be another power supply of 100V that will be used for generating high voltage magnitudes for the ultrasound pulser IC. There are a total of 9 different voltage levels that will need to be regulated; +100V, -100V, +12V, +10V, -10V, +5V, -5V, +3.3V, +1.8V. The design will consist of a buck converter, positive and negative linear regulators, and an inverting regulator.

A flow chart below depicts how the voltages will be regulated.

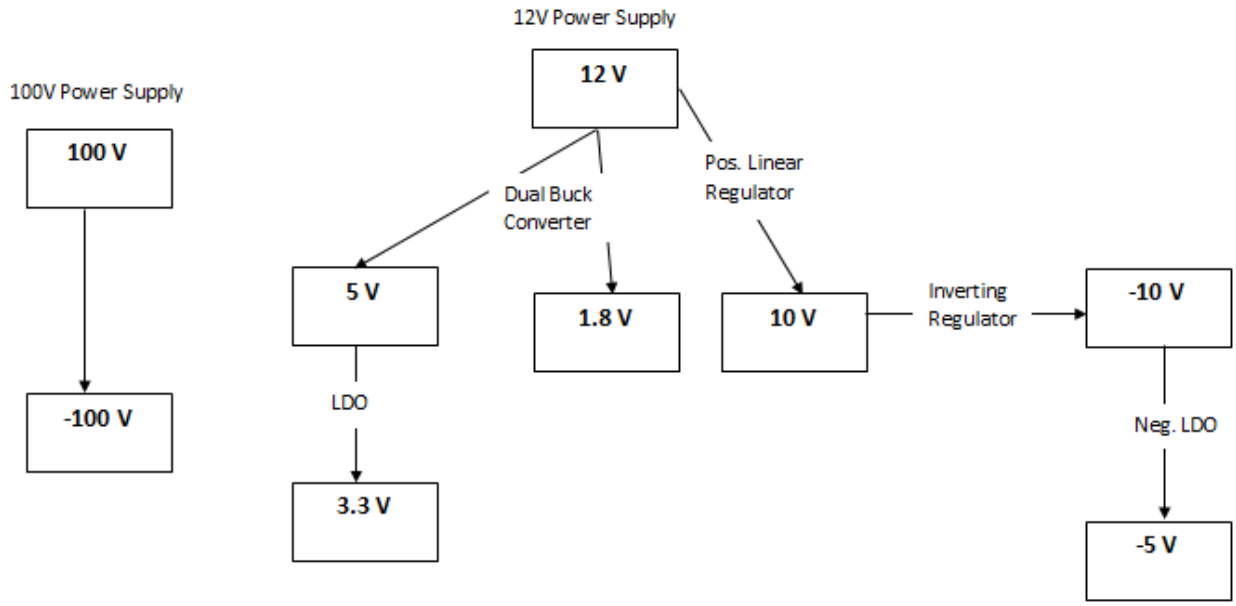

Figure 10: Power Flow Diagram

For the different power electronic components we chose Texas Instrument power regulating ICs. The components that were used are listed below:

- TPS54286 – Dual Buck Converter
- TPS7A4901 – Positive Linear Regulator
- TL497A – Inverting Regulator
- TPS7A3001 – Negative Linear Regulator
- TPS76933 – 3.3V Linear Regulator

100V Power Supply

The 100V power supply will connect with the Hitachi HV pulser. It will provide power for the positive and negative high voltage supply needed to amplify the incoming signals.

TPS54286 - Dual Buck Converter

The dual buck converter is used to regulate the 12V power supply to 5V and 1.8V. Texas Instruments provided schematics of external circuitry and the proper equations to select the external component values. A design procedure and external circuit set up was provided in the Texas Instruments datasheet. The procedure on selecting the external component values is followed by the schematic that is shown below.

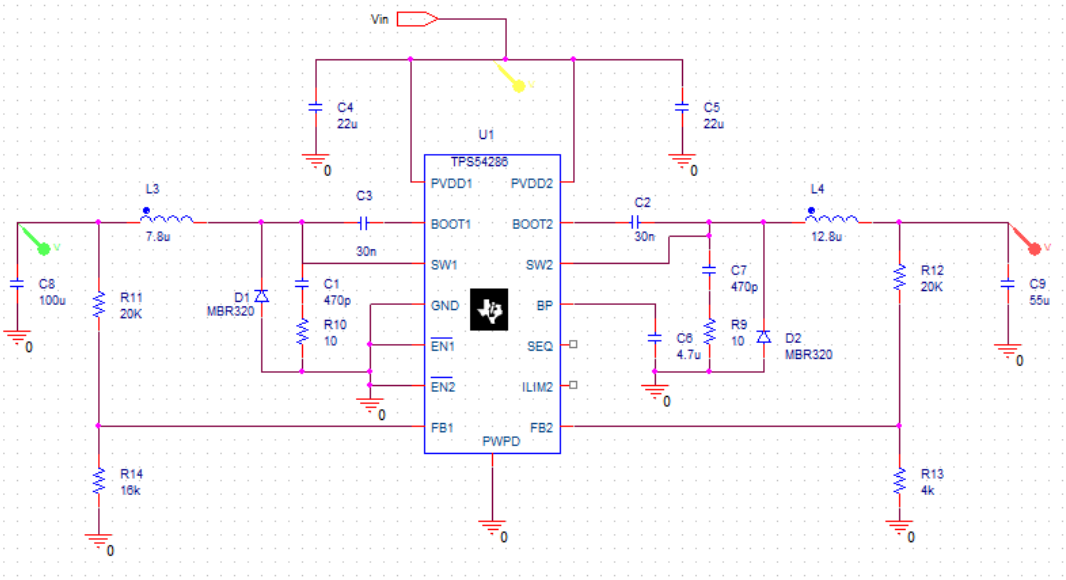

Figure 11: Dual Buck Converter Schematic

The minimum duty cycles of the circuit are described as:

$$D_{min} \approx \frac{V_{OUT} + V_{FD}}{V_{IN(max)} + V_{FD}}$$

The forward drop voltage, V_{FD}, for a schottky rectifier diode was assumed as 0.5V. Using the 5V and 1.8V output the minimum duty cycles were:

$$D_{5V,min} = \frac{5V + 0.5V}{12V + 0.5V} = 44\%$$

$$D_{1.8V,min} = \frac{1.8V + 0.5V}{12V + 0.5V} = 18.4\%$$

The inductor selection was governed by:

$$L_{min} \approx \frac{V_{IN(max)} - V_{OUT}}{I_{LRIP(max)}} \times D_{min} \times \frac{1}{f_{SW}}$$

The TSP54286 has a fixed switching frequency of *600kHz*. The maximum inductor ripple current is 600mA.

$$L_{5V,min} = \frac{12V - 5V}{600mA} \times 44\% \times \frac{1}{600kHz} = 12.8\mu H$$

$$L_{1.8V,min} = \frac{12V - 1.8V}{600mA} \times 44\% \times \frac{1}{600kHz} = 7.8\mu H$$

A schottky diode is selected as a rectifier diode for the low forward voltage drop. In the selection of the schottky diode the breakdown voltage we found the minimum voltage breakdown value.

$$V_{(BR)R(min)} \geq 1.2 \times V_{IN}$$

$$V_{BR,min} = 1.2 \times 12 = 14.4V$$

The diode must have a reverse breakdown voltage greater than 14.4V. A 20V device was used. The diode part number is MBRS320.

The output capacitor selection used the following equation:

$$C_{OUT} = \frac{1}{4 \times \pi^2 \times (f_{RES})^2 \times L}$$

The resonance frequency, f_{RES}, is about $6kHz$ for a ripple current of 600mA. The C_{OUT} values were calculated as follows:

$$C_{5V,OUT} = \frac{1}{4 \times \pi^2 \times 6000Hz^2 \times 12.8\mu H} = 55\mu F$$

$$C_{1.8V,OUT} = \frac{1}{4 \times \pi^2 \times 6000Hz^2 \times 78\mu H} = 90\mu F \rightarrow 100\mu F$$

The other capacitor values (i.e. the input, boot strap and BP) were given in the design example. This led us to selecting C4=C5=22µF, C2=C3=30nF, and C6=4.7µF.

The voltage setting feedback divider resistors, from V_{OUT} to FB, should range between 10kΩ and 50kΩ. A value of 20 kΩ was used for the R11 and R12 resistors. The selection of the R13 and R14 resistors used the following equations:

$$R13 = \frac{V_{FB} \times R12}{V_{OUT1} - V_{FB}}$$

$$R14 = \frac{V_{FB} \times R11}{V_{OUT2} - V_{FB}}$$

The forward bias voltage, V_{FB}, is given as 0.8V. Using those equations R13=3.83kΩ and R14=16kΩ. It is suggested that we add a RC snubber on the switch nodes to reduce the ringing. These values were given in the document as C1=C7=470pF and R9=R10=10Ω.

The designed circuit, along with the model of the TPS54286 IC was simulated in PSPICE. The transient analysis results are show below.

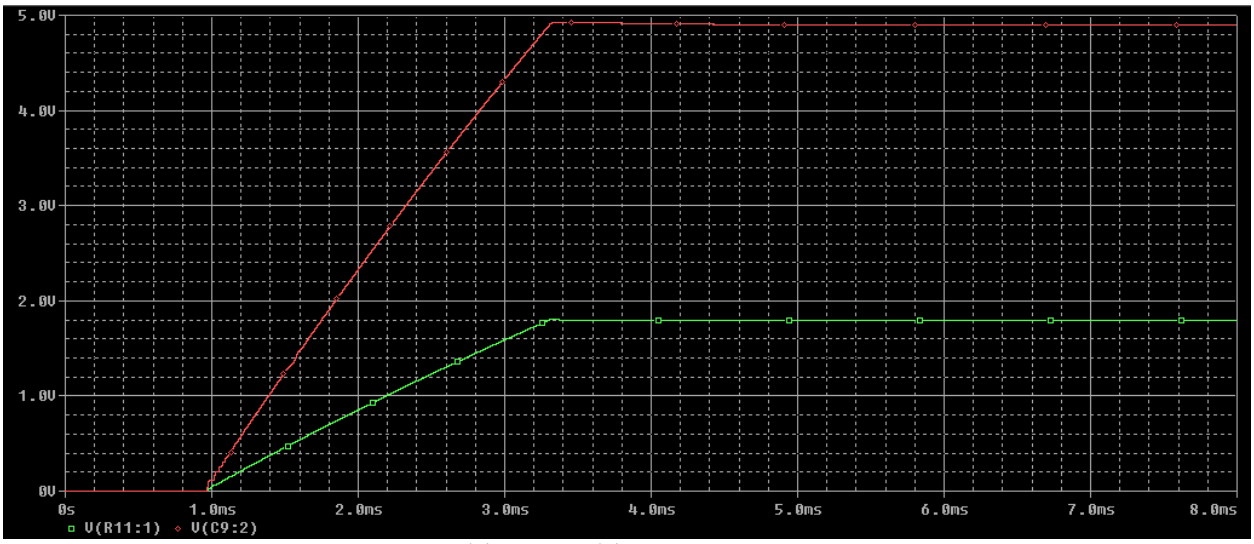

Figure 12: TPS54286 Transient Analysis Result

TPS7A4901 – Positive Linear Regulator

The positive linear regulator will be used to convert the 12V power supply voltage to 10V. Texas Instruments provided schematics of external circuitry and the proper equations to select the external component values. A design procedure and external circuit set up was provided in the Texas Instruments datasheet. The procedure on selecting the external component values is followed by the schematic that is shown below.

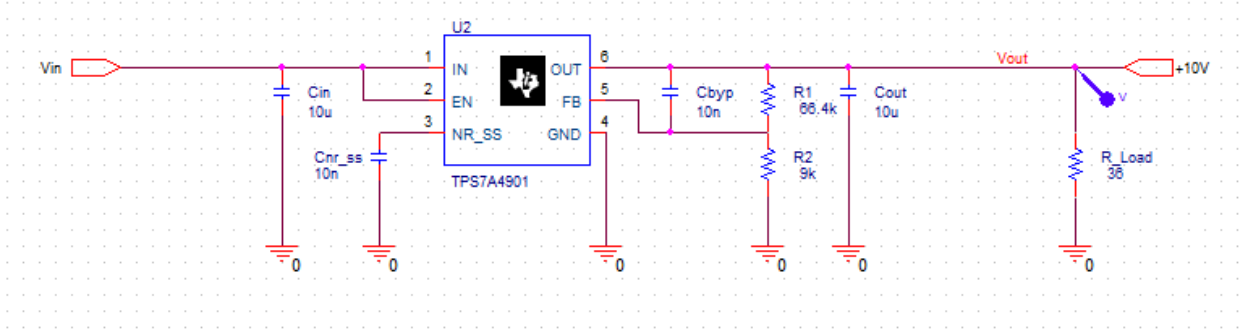

Figure 13: Positive Linear Regulator Schematic

The output voltage and the voltage divider equations were provided as:

$$R_1 = R_2\left(\frac{V_{OUT}}{V_{REF}} - 1\right), \quad \text{where } \frac{V_{OUT}}{R_1 + R_2} \geq 5\mu A$$

V_{REF} is the internal reference voltage and it is 1.194V. Selecting a R_2 resistance of 9kΩ yields a R_1 resistance of 66.4kΩ.

In selection of the input and output capacitors, we chose the values that Texas Instruments suggested in the datasheet. The noise and bypass capacitors are not needed, but they are recommended in the datasheet to minimize noise and maximize AC performance.

The designed circuit of the TPS7A4901 was simulated in PSPICE. The transient results are shown below.

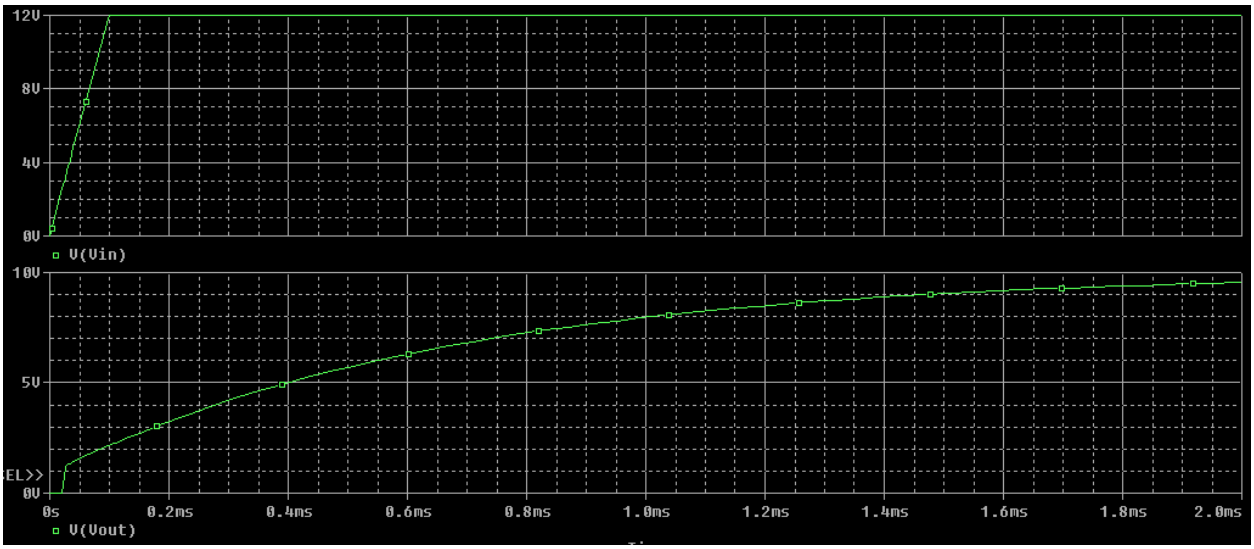

Figure 14: TPS7A4901 Transient Analysis Result

TL497A – Inverting Regulator

The inverting regulator will be used to convert 10V to -10V. Texas Instruments provided schematics of external circuitry and the proper equations to select the external component values. A design procedure and external circuit set up was provided in the Texas Instruments datasheet. The procedure on selecting the external component values is followed by the schematic that is shown below.

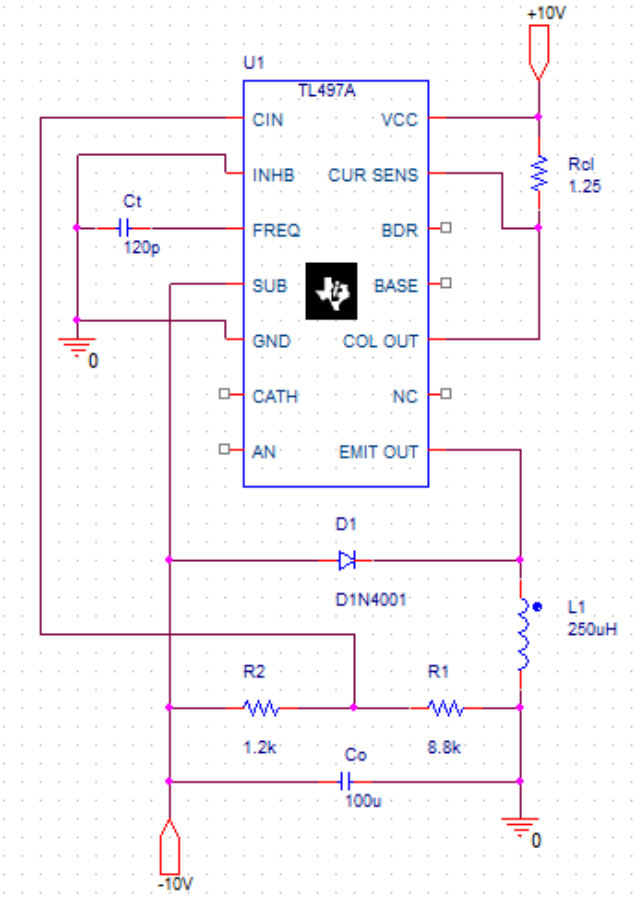

Figure 15: Inverting Regulator Schematic

The following equations were provided from the Texas Instruments datasheet. These equations were used in the design of the external circuit.

$$I_{(PK)} = 2\,I_O \max\left[1 + \frac{|V_O|}{V_I}\right]$$

$$L\,(\mu H) = \frac{V_I}{I_{(PK)}} t_{on}(\mu s)$$

$$C_T(pF) \approx 12\,t_{on}(\mu s)$$

$$R1 = \left(|V_O| - 1.2\,V\right) k\Omega$$

$$R_{CL} = \frac{0.5\,V}{I_{(PK)}}$$

$$C_O\,(\mu F) \approx t_{on}(\mu s) \frac{\left[\frac{V_I}{|V_O|} I_{(PK)} + I_O\right]}{V_{ripple}\,(PK)}$$

There were suggested values in the datasheet that were used in the design of the circuit. The suggested values were I_o=100mA, $V_{RIPPLE(PK)}$=50mV, R_2= 1.2kΩ, V_I=10V, V_O=-10V, and t_{ON}=10µs. Using these values yielded $I_{(PK)}$=0.4A, L=250µH, C_T=120pF, R1=8.8kΩ, R_{CL}=1.25Ω, and C_O=100µF.

TPS7A3001 – Negative Linear Regulator

The negative linear regulator will be used to convert the -10V to -5V. Texas Instruments provided schematics of external circuitry and the proper equations to select the external component values. A design procedure and external circuit set up was provided in the Texas Instruments datasheet. The procedure on selecting the external component values is followed by the schematic that is shown below.

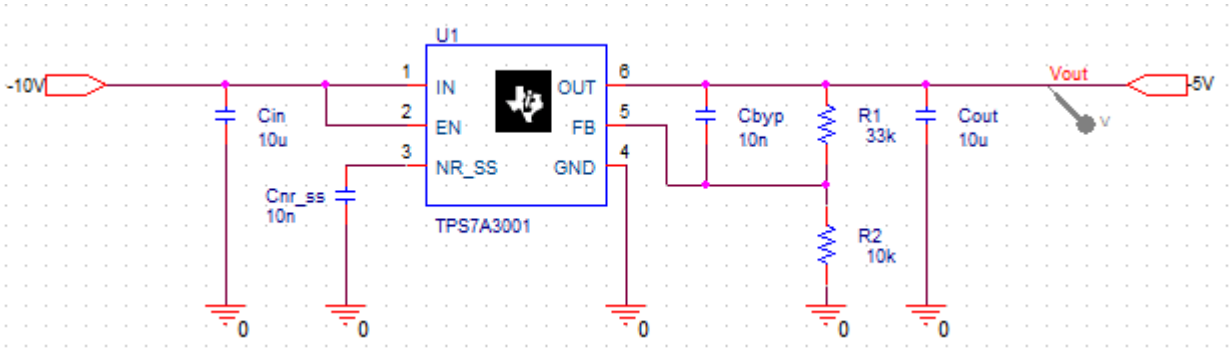

Figure 16: Negative Linear Regulator Schematic

The negative linear regulator used the same equations as the positive linear regulator. The voltage equations provided in the Texas Instruments datasheet are shown below.

$$R_1 = R_2\left(\frac{V_{OUT}}{V_{REF}} - 1\right), \quad \text{where } \frac{V_{OUT}}{R_1 + R_2} \geq 5\mu A$$

V_{REF} is the internal reference voltage, and it is -1.184V. Selecting a R_2 resistance of 10kΩ yields a R_1 resistance of 33kΩ.

The designed circuit of the TPS7A3001 was simulated in PSPICE. The transient results are shown below.

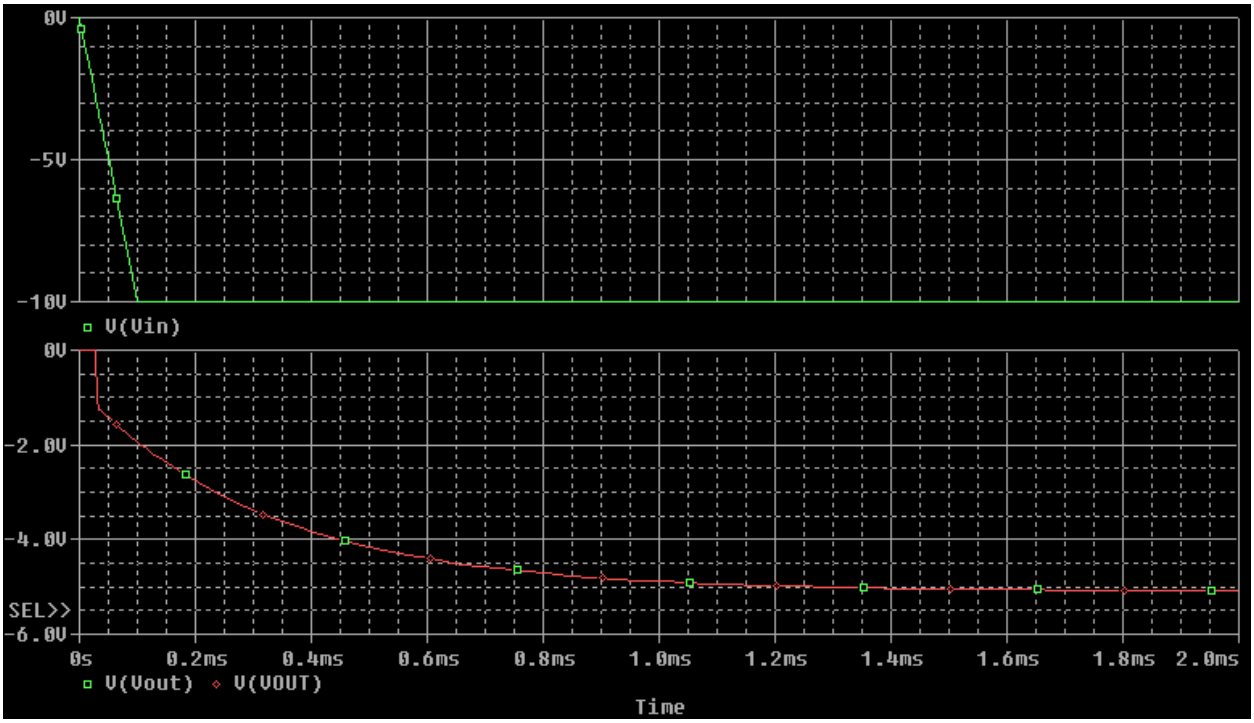

Figure 17: TPS7A3001 Transient Analysis Result

TPS76933 – 3.3V Linear Regulator

The 3.3V linear regulator will be used to convert 5V to 3.3V. There was no design procedure for this IC, since it is a fixed output regulator. The only external circuitry used was one input capacitor and one output capacitor. Texas Instruments datasheet suggested that the input capacitor be 1µF and the output capacitor be 4.7µF. The schematic is shown below.

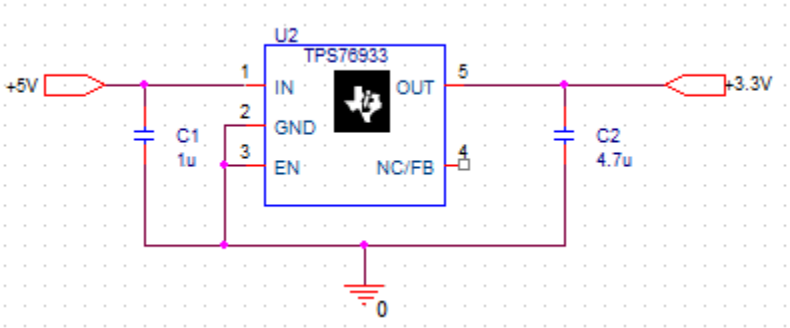

Figure 18: 3.3V Linear Regulator

Testing and Evaluation Plan

Due to many of the parts used in the design not having PSPICE model files, our team is planning to order the parts and design simple test circuits in order to confirm proper functionality and design of interfaces. The test plan for each device along with design information regarding test boards is given below.

1. **Transmitter Test Plan**
   Since the transmitter has a significant amount of hardware, the test board must be able to verify the functionality of each component individually to help with debugging. Due to the danger of high-voltages, the order for which devices will be tested is given below:

   1. Test the functionality of the Integrated switch bank
   2. Test the functionality of the TX810 according to the procedure below
   3. Test the functionality of the HV Pulser according to the procedure below

   HV Pulser

   1. The Logic inputs must be tested to ensure that the FPGA can control the device effectively.
      a. Apply logic power signals to the Hitachi pulser
      b. Apply a low-voltage 5-10V signal to the VPP and VNN inputs (through the power connector on the board)
      c. Apply logic signals to the inputs and observe the output pin voltage values, ensure that the values meet expectations.
      d. Once the basic functionality is confirmed, higher voltages can be supplied to the device and faster switching can be tested
   2. Output Signal Must be measured with an Oscilloscope to ensure the waveform is correctly generated
      a. Once the device is configured correctly, the inputs can be controlled such that a realistic signal is generated (i.e. the output signal is above 3MHz and the supply voltage can be varied 0-100V)
   3. Output currents must be measurable to get an accurate measure for how much current the system will draw
      a. Tap points must be present in the line in order to connect a multimeter.

   Integrated Switch Bank

   1. Confirm that the correct logic supply voltages are generated before applying to the circuit.
   2. Confirm the control interface for the device works correctly
      a. Apply the logic power supply
      b. Supply the device with a serial input signal, clock signal, and LE signal to control the configuration of active switches in the bank
      c. Measure connectivity of switch outputs with multimeter to ensure that switches are accurately controlled
   3. Once basic functionality is confirmed, apply high-voltage supplies and confirm functionality
      a. Follow the same basic procedure as Step 2
   4. Test the device with the Hitachi pulser inputs
      a. Measure the outputs of the switches to ensure that high-voltage pulses are passed through the device

TX810 Transmit/Receive Switch

1. Confirm that all power supplies are generating correct voltage levels before applying to the circuit
2. Confirm that the control pins are receiving the proper signals
    a. Measure tap points with a multimeter
3. Apply the high-voltage signal and measure the output, ensure that no HV transients are allowed through the device.

2. Receiver Test Plan

Due to the analog front end making up most of the receive circuit, receive circuit testing will revolve around the analog front end IC.

Analog Front End

1. The data stream on the AFE5808 must be checked
    a. Verify with a time domain test that can be conducted in the GUI. A procedure for accomplishing this can be found in the User Guide for the AFE5808 Evaluation Module.
2. Verify continuous mode
    a. Apply a small-signal voltage source and collect the sampled data to a computer interface. The samples should match the data that was transmitted through the AFE EVM.
3. Verify the External ADC Sampling Clock
    a. Reconfigure jumpers
    b. Apply a generator output of 40 MHz and measure the signal in an oscilloscope.

3. Power Electronics Testing

To test power regulation a test board must be built. The test board will allow us to test the regulation of the individual components and the external circuitry. There will be tests of individual components and the components combined together. PSPICE simulations were done for the components that had available PSPICE model files.

12VDC Power supply

Requirements

1. 12VDC must be supplied from power source.
2. Power supply connected to Dual Buck converter.
3. Power supply connected to Positive Linear Regulator.

Test

1. Output of power supply is measured at 12VDC.
2. 12VDC is measured at Dual Buck Converter input, PVDD1 & PVDD2.
3. 12VDC is measured at Positive Linear Regulator input Vin.

Dual Buck Converter

Requirements

1. The Dual Buck converter must regulate an output voltage of 5V.
2. The Dual Buck converter must regulate an output voltage of 1.8V.
3. 5V output must connect to the 3.3 Linear Regulator input.
4. 5V output must connect to HV pulser pin Vdd.
5. 5V output must connect to T/R switch pin Vp.
6. 1.8V output must connect to AFE pin AVDD18.
7. 1.8V output must connect to AFE pin DVDD18.

Test

1. Output of dual buck is measured at 5V.
2. Output of dual buck is measured at 1.8V.
3. 5V is measured at the 3.3V LDO input pin.
4. 5V is measured at the HV pulser Vdd pin.
5. 5V is measured at the T/R switch Vp pin.
6. 1.8V is measured at the AFE AVDD18 pin.
7. 1.8V is measured at the AFE DVDD18 pin.

Positive Linear Regulator

Requirements

1. The positive linear regulator must regulate an output voltage of 10V.
2. 10V output must connect to the Inverting Regulator input.
3. 10V output must connect to the HV pulser pin Vdd12.

Test

1. Output of positive linear regulator is measured at 10V.
2. 10V is measured at Inverting regulator input.
3. 10V is measured at the HV pulser Vdd12 pin.

Inverting Regulator

Requirements

1. The inverting regulator must regulate an output voltage of -10V.
2. -10V output must connect to the negative linear regulator.
3. -10V output must connect to the HV pulser pin Vss.

Test

1. Output of inverting regulator is measured at -10V.
2. -10V is measured at negative linear regulator input pin.
3. -10V is measured at the HV pulser Vss pin.

Negative Linear Regulator

Requirements

1. The negative linear regulator must regulate an output voltage of -5V.
2. -5V output must connect to the HV pulser Vdd pin.
3. -5V output must connect to the T/R switch pin Vn.

Test

1. Output of negative linear regulator is measured at -10V.
2. -5V is measured at the HV pulser Vdd pin.
3. -5V is measured at the T/R switch Vn pin.

3.3V Linear Regulator

Requirements

1. 3.3V linear regulator must regulate an output voltage of 3.3V.
2. 3.3V output must connect to HV pulser pin VLL.
3. 3.3V output must connect to AFE pin AVDD3.
4. 3.3V output must connect to T/R switch pin Vd.

Test

1. Output of the 3.3V linear regulator is measured at 3.3V.
2. 3.3V is measured at the HV pulser VLL pin.
3. 3.3V is measured at the AFE AVDD3 pin.

3.3V is measured at the T/R switch Vd pin.

Standards

The best source an industry standard for Ultrasounds was in the Code of Federal Regulations under section number 21 CFR 1050.10. It firsts explains all the definitions that are needed to understand the material and then goes into some performance requirements. I have listed the requirements that apply to us below:

1. A means shall be incorporated to indicate the magnitudes of the temporal-average ultrasonic power and the temporal-average effective intensity when emission is of continuous-wave waveform.
2. A means shall be incorporated to enable the duration of emission of ultrasonic radiation for treatment to be preset and such means shall terminate emission at the end of the preset time. Means shall also be incorporated to enable termination of emission at any time. Means shall be incorporated to indicate the magnitude of the duration of emission.
3. A means shall be incorporated for indicating the magnitudes of pulse duration and pulse repetition rate of the emitted ultrasonic radiation, if there are operation controls for varying these quantities.
4. A means shall be incorporated to provide a clear, distinct, and readily understood visual indicator when and only when electrical energy of appropriate ultrasonic frequency is being applied to the ultrasonic transducer.

The next sub index of this section describes where and how labels should be fixed to the ultrasound. All of the controls need to have a label explaining what each control does and how to use it. The waveform generator must also have a label fixed on it. The specifications for labels are listed below:

> Labels required by this paragraph shall be permanently affixed to or inscribed on the ultrasonic therapy product; they shall be legible and clearly visible. If the size, configuration, or design of the ultrasonic therapy product would preclude compliance with the requirements of this paragraph, the Director, Center for Devices and Radiological Health, may approve alternate means of providing such labels.

The last part of this section explains what information must be explained by the manufacturer of the ultrasound. It is listed below:

1. Adequate instructions concerning assembly, operation, safe use, any safety procedures and precautions that may be necessary regarding the use of ultrasonic radiation, and a schedule of maintenance necessary to keep the equipment in compliance with this section.

2. Adequate description of the spatial distribution of the ultrasonic radiation field and the orientation of the field with respect to the applicator. This will include a textual discussion with diagrams, plots, or photographs representative of the beam pattern.
3. Adequate description, as appropriate to the product, of the uncertainties in magnitude expressed in terms of percentage error, of the ultrasonic frequency effective radiating area, and, where applicable, the ratio of the temporal-maximum effective intensity to the temporal-average effective intensity, pulse duration, pulse repetition rate, focal area, and focal length.
4. A listing of controls, adjustments, and procedures for operation and maintenance, including the warning "Caution—use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous exposure to ultrasonic energy."

These standards produced by the federal government ensure that the ultrasound is used properly.

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