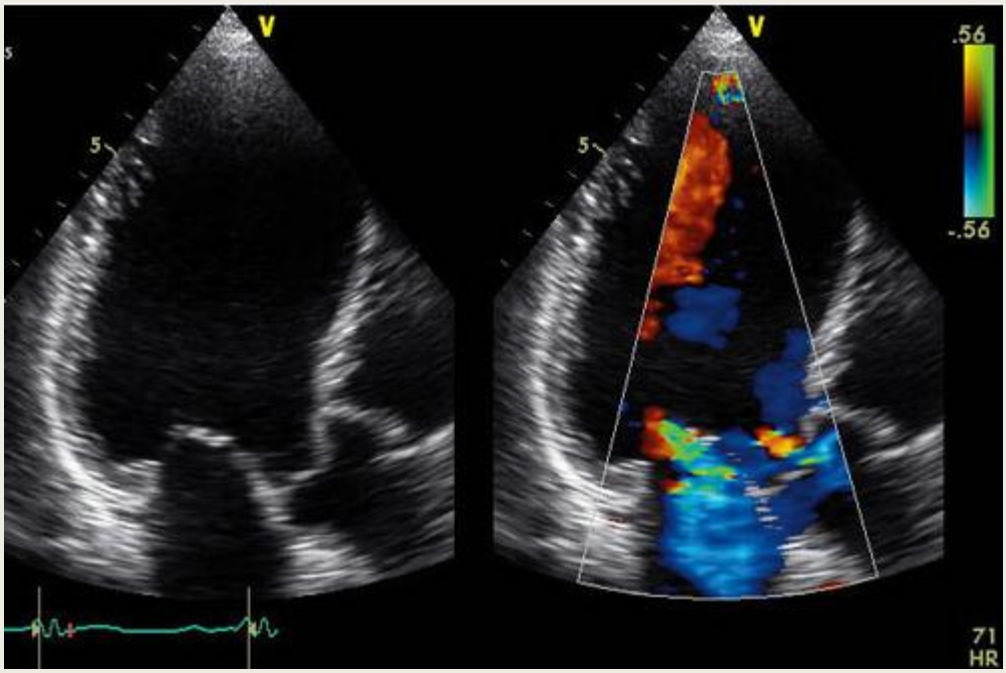
February 2012

Dr. Tim Bigelow

Pulse-Echo Ultrasound Final Design Document



http://www.gehealthcare.com/euen/ultrasound/products/cardiovascular/vivid-q/index.html

Dec2012-04 | Allen Kellar, Amairani Tapia, Francis Ferrer, Justin Batcheler, Jon Driggs, Richard Page

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Introduction

The objective of this project was to create a Pulse-Echo Ultrasound transmitter to image the brain. This paper will describe our course of action for completing this ultrasound system in the two semesters provided. The first part of this report consists of the project plan and an explanation of: the time management, expenses, and resource requirements. The design information begins on page 10 and focuses on the specifics of each component, how they interact with each other, and actual implementation.

Table of Commonly Used Terms

Term	Meaning
"Pulser"	A device that can provide square wave pulses
"High Voltage" or "HV"	A voltage level ranging form 20V to 100V
"Analog Front End"	A device made by Texas Instruments that incorporates all the necessary hardware to recover ultrasound signals into one package.
"Multiplexing"	Switching a small number of inputs amongst a larger number of outputs

Problem Statement

In order to understand the project, a brief description of brain-imaging technology will be given. One technology that will be evaluated is fMRI. Functional magnetic resonance imaging (fMRI) is a noninvasive test that uses a strong magnetic field and radio waves to look at blood flow in the brain and detect areas of activity. Oxygen-rich blood and oxygen-poor blood have a different magnetic resonance. The most active areas of our brain receive more oxygenated blood. The advantage in fMRI is that it does not emit radiation like X-rays, computed tomography, and positron emission tomography scans. Although the fMRI is a very effective brain-imaging system, it is also very expensive. In Lieu of such high costs, the design of a pulse echo ultrasound system was pursued. A pulse echo system consists of a transducer assembled with 128 small individual elements that can each be pulsed separately. The purpose of pulsing each element separately is to allow for a phased-array of signals (signals with different phases ranging from 10ns to 20us) to be sent through the ultrasound probe. Additionally, pulse echo ultrasound millions of pulses and echoes are sent and received each second. These sound waves are reflected back to the probe once a boundary between tissues is found, and the reflected signals can be processed to form an ultrasound image.

An ultrasound circuit is composed of many parts that serve different functions. The design that is being used has eight major components that define the circuit. The components are as follows: waveform generator, high voltage amplifiers, transmit/receive circuit, ultrasound transducer, low-noise amplifiers, and variable-gain amplifiers. A block diagram of the system is shown below in Figure 1 where you can see the relations of the components.

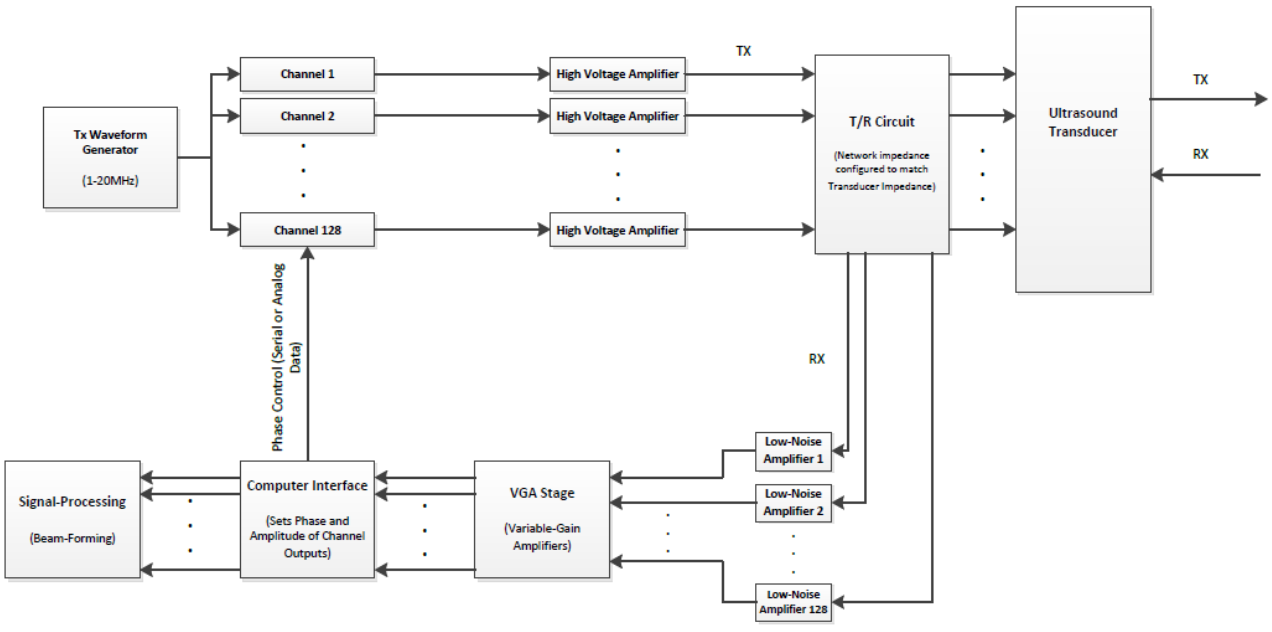


Figure 1 – General Block Diagram of the Ultrasound System

A brief description of each system component shown in the block diagram is given below.

Waveform Generator

The waveform generator generates digital samples of 3 MHz ultrasound pulses. A high-speed DAC will be used to convert the digital waveforms to the analog domain. In total, 128 individual signals will be generated by this functional block.

High Voltage Amplifier

High voltage amplification of the generated pulses is necessary in order to provide enough energy to the ultrasound transducer (due to poor electrical to acoustic energy conversion within the transducer). A stronger signal means that there is less opportunity for signal loss while being transmitted. The maximum voltage that this component will generate is 100 VDC, or 200V peak-peak.

Transmit/Receive Circuit

The transmit/receive circuit will transmit the amplified pulses to the ultrasound transducer. It will receive the reflected low voltage signals from the transducer and use them for the signal processing of the ultrasound. The transmit/receive circuit will also prevent high-voltage pulses from entering the receiver circuitry.

Low-Noise Amplifier

The low-noise amplifier will amplify the weak reflected signals that the transmit/receive circuit receives from the ultrasound transducer. It's placement after the receiver is to recover the low-power reflected ultrasonic signal in the presence of significant noise.

Variable-Gain Amplifier

A variable-gain amplifier is placed after the low-noise amplifier and is used to map the signal into the appropriate dynamic range for signal processing. Computerized control of this device will allow for the gain to be adjusted appropriately over time.

Computer Interface

A computer interface will be used to control the phase and magnitude of the waveform generator channel outputs. The delay range is 10 ns – 20 us. Additionally, recovered signals will be sent to the computer interface for signal processing and recovery.

Signal Processing

Recovered (reflected) ultrasound pulses will be amplified and communicated to the computer interface for digital signal processing and imaging. All signal processing will be done in the computer interface.

Transducer

The transducer, otherwise known as the probe, is the component in the system that has contact with the body. The basic function of the transducer is to receive an electrical pulse and convert it into a acoustic vibration at a pre-determined frequency. Ultrasonic pulses reflected off of the body are captured by the transducer and converted into electrical signals that can be processed to form images.

Resource requirements

The technical requirements, system requirements, and user interface requirements are given in the tables below. Highlighted text indicates that the information is unknown at this point.

Table 1 - Resource Requirement Descriptions

System Component:	Requirement Description:
Waveform Generator	The waveform generator shall be capable of controlling the pulser integrated circuits in order to produce high-voltage signals. Each output must be individually controllable in order to implement a phased-array system.
Waveform Generator	The waveform generator shall be capable of being controlled by the user interface.
High Voltage Amplifier (Pulser)	The high voltage amplifier shall be capable of amplifying the input waveform so the output has a pulse amplitude 190 Vpp.
High Voltage Amplifier (Pulser)	The amplifier circuit shall have a bandwidth that exceeds 3 MHz.
T/R Circuit	The T/R circuit shall function as protection against high-voltage transients for the receiver. However, the T/R circuit shall allow high-voltage transmitted signals to propagate to the Ultrasound Transducer.
T/R Circuit	The T/R circuit shall only allow a signal with maximum amplitude of X V to enter the receiver circuit.
T/R Circuit	The T/R circuit shall have impedance matching with the Ultrasound Transducer. (Note: Ultrasound Transducer Electrical Characteristics are unknown at this point)
Analog Front End	The Analog Front End shall contain a low-noise amplifier to recover a small-magnitude signal from the transducer output.
Analog Front End	The Analog Front End shall contain a variable gain amplifier with an adjustable gain.
Analog Front End	The Analog Front End shall contain an ADC capable of sampling at 50MSPS and that produces serial LVDS data at the output.

Transducer	Operates in the 3 MHz frequency range
Transducer	Linear array with 128 elements

Market and Literature Survey of Similar Products

Ultrasound technology has quickly advanced in the past 20 years due to the introduction of high-power processing and cheaper, more complex integrated circuit components. Modern ultrasound systems are designed by companies with very experienced teams of engineers who rarely share proprietary design information. Therefore, our team began our project by researching how an ultrasound system works at a system-level. Once the overall functionality of the system was understood, we searched for existing patents on individual functional blocks of the system. Useful information was found for: High-voltage pulse generation, transmit/receiver circuitry, digital beam forming, and reflected signal recovery (see the block diagram for reference of the system components listed). Additionally, our client Dr. Bigelow provided us with a product guide from a existing ultrasound system that lists some of its technical specifications (such as minimum time delay and peak waveform amplitude).The technical specifications we gathered from the product guide were incorporated into our project requirements.

Several patents and research papers that have been referenced extensively are given below.

[1] Koen, Myron. "Ultrasound Transmitter." *United States Patent Application Publication* May 6, 2010. 1-9. *United States Patent Database*. Web. 2 Feb 2012.

[2] Udpa, Satish. "Apparatus and Method for Driving an Ultrasonic Transducer." *United States Patent Application Publication* June 3, 1997. 1-9. *United States Patent Database*. Web. 2 Feb 2012.

[3] Camacho, Jorge, and Carlos Fritsch. "Protection Circuits for Ultrasound Applications." *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control* 55.5 May 2008. 1160-1164. *IEEE.* Web. 5 Feb 2012.

[4] Hatfield, J V, P A Payne, and N R Scales. "Transmit and Receive ASICs for an Ultrasound Imaging Multi-Element Transducer." *IEEE* (1994): 1-9. *IEEE*. Web. 13 Feb 2012.

[5] Poulsen, Jens. "Low Loss Wideband Protection Circuit for High Frequency Ultrasound." *IEEE Ultrasonics Symposium* 823-826. *IEEE*. Web. 13 Feb 2012.

Issues

The issues that the project faced were mainly due to the grand scale of the project itself. The main circuit that was designed had 6 layers and would cost around $900, a couple hundred dollars over the budget. After

the extra funds were approved by the department, the circuit was ordered on 12/3/2012. Problems also occurred when testing some of the components. The pulser could not complete testing because some apparatuses malfunctioned and could not be replaced in time. The power electronics simply did not have some of the materials that it needed that were test-ready.

Estimated Costs

Part:	Part Description:	Cost:
ML605 Evaluation Kit	XLINX FPGA Board	$1,800
FMC XM101 LVDS QSE Mezzanine Card	FPGA breakout board for LVDS pins with QSE Connectors	$700
AFE5808EVM	Analog Front End Analog to Digital Converter Evaluation Board	$299 x 6= $1,794.00
TSW1250EVM	Analysis system	$650.00
TX810	Transmit/Receive Switch	$11.16 x 10 = $111.60
HDL6V5581	HV Pulser	$0
MAX14803CCM	High-Voltage Switch Bank	$26.91 x 14 = $376.74
Ultrasound Probe		$15,000.00
Power Electronics	Regulators and Converters	$320.19
Resistors, Capacitors, Inductors		$173.86
Connectors	Transducer and Mezzanine card connectors	$264.03
PCB Fabrication		$1000
Total Cost		$22,190.42

Table 2 - Estimated Cost of Hardware

The table above lists the hardware that has been purchased for our ultrasound prototype. In order to reduce costs and development time, we have chosen to implement a 32-channel system and multiplex the 128 outputs of the ultrasound probe to the system using a MAXIM high-voltage switch bank.

Project Schedule

This project took place over the course of two semesters. During the first semester, the main focus was project planning and design. During the second semester, our focus shifted to testing and implementing our engineered circuit, creating the printed circuit boards, and ordering parts as we saw necessary. The following dates provide a timeline for the schedule we have followed. Note that the final design was revised due to high PCB fabrication costs.

Task	Details	Start	Finish	Duration
Problem Definition	Meet with advisor; Gain understanding of the project.	1/9/2012	1/13/2012	4 Days
Research	Research patents on ultrasound systems.	1/16/2012	2/17/2012	32 Days
Identify Circuit Components	Research components and different technologies; select components that will be used.	2/1/2012	3/30/2012	59 Days
Initial Design	Design a 1 channel circuit.	3/1/2012	4/9/2012	40 Days
PSPICE Simulation	Test and verify available model files to ensure theoretical functionality.	3/15/2012	4/20/2012	36 Days
Final Design	Expand the 1 channel circuit into 32 channels. Implement switching scheme.	4/9/2012	4/27/2012	19 Days
Order Parts	Order selected components.	4/2/2042	6/12/2012	60 Days
PCB Layout	Create the PCB layouts for the system.	9/3/2012	11/5/2012	63 Days
FPGA Programming	Program FPGA for input signals.	9/1/2012	10/27/2012	57 Days
Physical Breadboard	Create physical breadboard prior to PCB creation.	9/10/2012	10/29/2012	49 Days
Breadboard Testing	Test breadboard components. (Power electronics and HV Pulser.)	10/12/2012	11/2/2012	33 Days
Design Revision	Revise the 32 channel switching design into 16 channel design.	11/14/2012	11/16/2012	4 Days
PCB Layout Revision	Revise PCB layouts to reflect new design.	11/16/2012	11/22/2012	6 Days

Order Parts	Order new parts that are needed/missing.	11/19/2012	11/26/2012	7 Days
Fabricate Final PCB	Order the final PCB to get fabricated.	11/26/2012	-	

Table 3 – Project Schedule

System Analysis

Ultrasound technology has rapidly evolved in the past few decades. Several large companies such as Texas Instruments and Maxim have extensive portfolios of ultrasound-specific integrated circuit products. Our team elected to primarily use Texas Instrument products, due to the fact that Texas Instruments is willing to donate products and services to senior design teams.

In order to select the different components we need for our system, we followed the suggestions of the following flow-chart provided on Texas Instruments' website:

[REF] http://www.ti.com/solution/ultrasound_system

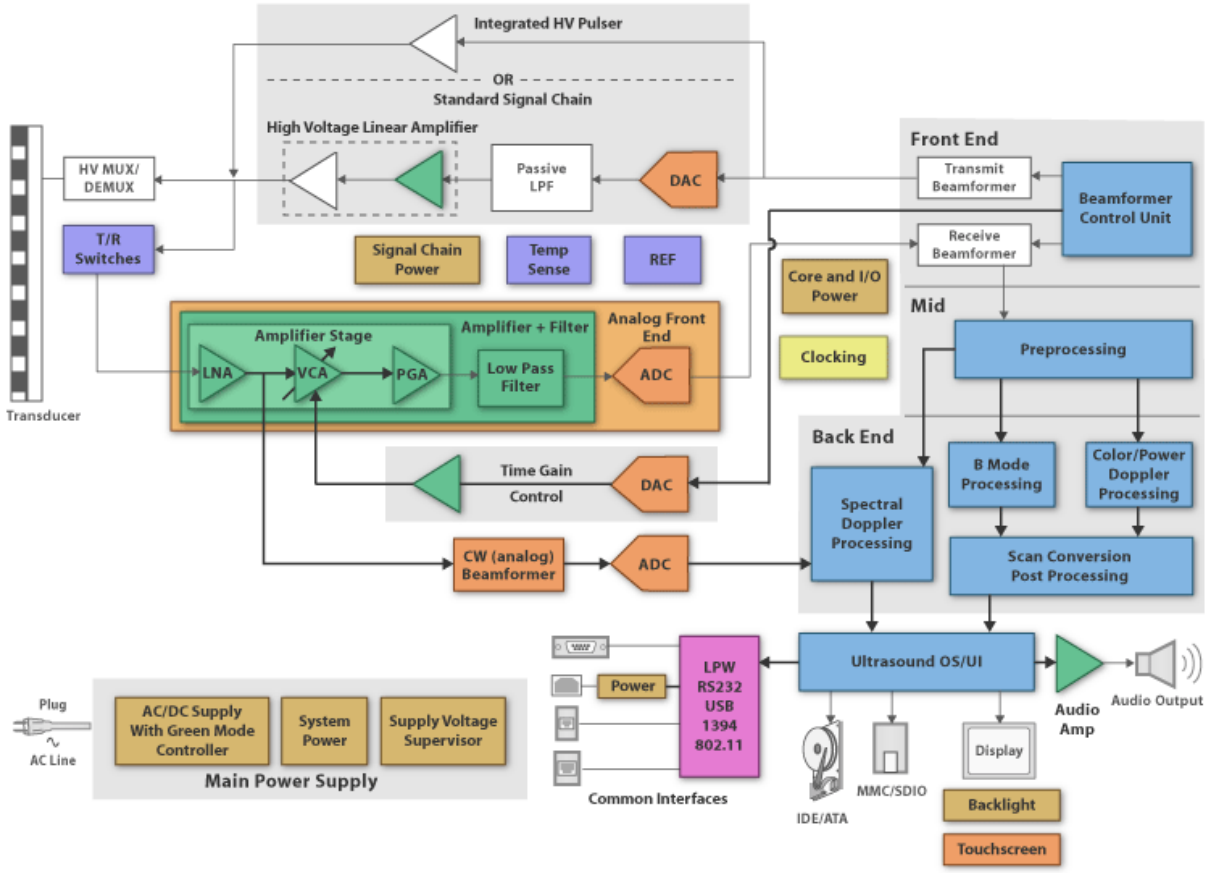


Figure 1 - Block Diagram with Suggested Texas Instruments Products

Using this flow-chart, we selected the following products to use for our design:

- TX810 – Integrated T/R Switch
- AFE5808 – Analog Front-End Integrated Circuit
- Texas Instruments Voltage Regulators

Out of all the components listed above, the most consideration was placed into the component to be used for digital waveform generation and acquisition. At first, our team assumed that ADC and DAC cards with 32-128 I/O pins would be readily available in the market with the specifications we desired. However, after contacting several vendors, it was determined that there is no cost-effective solution to implementing these functions with existing products. Therefore, we have decided to use a XLINX FPGA development board to perform signal generation and transmitter control operations.

Details for each component and its electrical characteristics are given in the "Detailed Design" portion of this document. Comments regarding functionality and design trade-offs for each component are also given in the "Detailed Design" portion of this document.

Ultrasound Transmitter Design

The detailed design information for the ultrasound system is given in this section. The entire design is broken down into individual functional parts in order to increase readability and understanding. A detailed block diagram of the transmit circuit is included in Figure 5 in order to give better insight into the entire design, and should be referenced to clarify confusion regarding system architecture. This diagram gives a description of interfaces between the following functional blocks:

- Waveform Generation (FPGA Platform)
- High Voltage Pulser
- Output Multiplexing (Integrated Switch Banks)

Each of the functional blocks listed (Waveform Generation, High Voltage Pulser, and Output Multiplexing) is described below in greater detail. Descriptions of the devices and components selected to perform each function are also given. Once all of the functional blocks have been described, the overall transmit block diagram in Figure 5 is introduced to give insight into the architecture of the entire system.

Waveform Generation

The waveform generation for the ultrasound system will be accomplished by using an XLINX ML605 FGPA development board. Specifically, this FPGA board will provide logic control for the pulser integrated circuits (described in the next section). The FGPA board will also control the interface between the circuitry and the ultrasound transducer, which is described in the section "Output Multiplexing". The table below describes the important specifications of the FPGA board and relates them to the system requirements for the waveform generation functional block.

Parameter	Device Specification	Required Specification
Output Signaling Speed	Up to 7GHz	50-100MHz
Programmability and Debugging Interface	Easily programmable through a ISE Design Suite	Programmable through a computer interface
Outputs	2 FMC Connectors: The first is a high pin count	64 I/O pins that can be used to control the pulser logic inputs.

	(HPC) configuration that provides connectivity for 160 single-ended or 80 differential user-defined signals. The second is a low pin count (LPC) configuration that provides connectivity for 68 single-ended or 34 differential signals.	
Expandable Memory Option	Included	Desired

The table illustrates that the FGOA board is appropriate for our purposes.
The XLINX ML605 FPGA evaluation board is shown below in Figure 2.

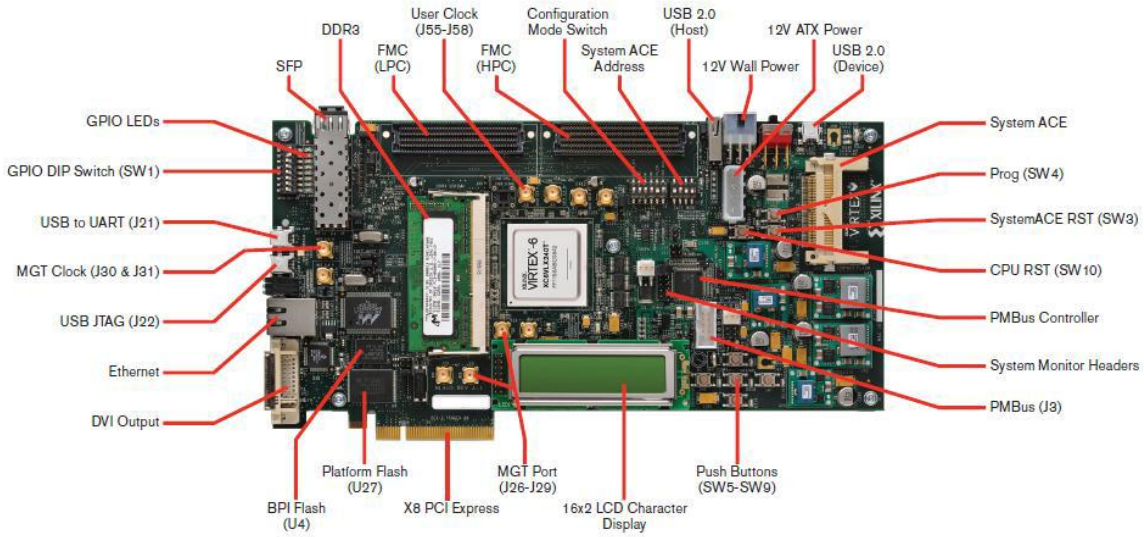


Figure 2 - Image of FPGA Evaluation Board

Once the evaluation board shown in Figure 2 is received, the following items will be thoroughly tested:

- Output signaling interface to pulser inputs
- programmability
- confirm the number of available outputs

Once the functionality of the device is confirmed, the device will be used to drive a 32-channel ultrasound system transmitter circuit.

High Voltage Pulser

High voltage switching will be accomplished by using an integrated circuit designed specifically for the task. Hitachi semiconductor has an extensive line of ultrasound-specific integrated circuits, and we will utilize the HDL6V5581. The essential specifications for the device are listed in the table below.

Parameter	Device Specification	Required Specification
Bipolar output voltage limits	+/- 105V	+/-100V
Frequency Range of Operation	1 MHz – 25 MHz	3 MHz
Number of Channels	8	4-32 channels desired
Switching Delay Time	24ns	Less than 167ns

The HDL6V5581 will be utilized using the circuit shown below (note: only input and output pin interfaces are detailed in Figure 3:

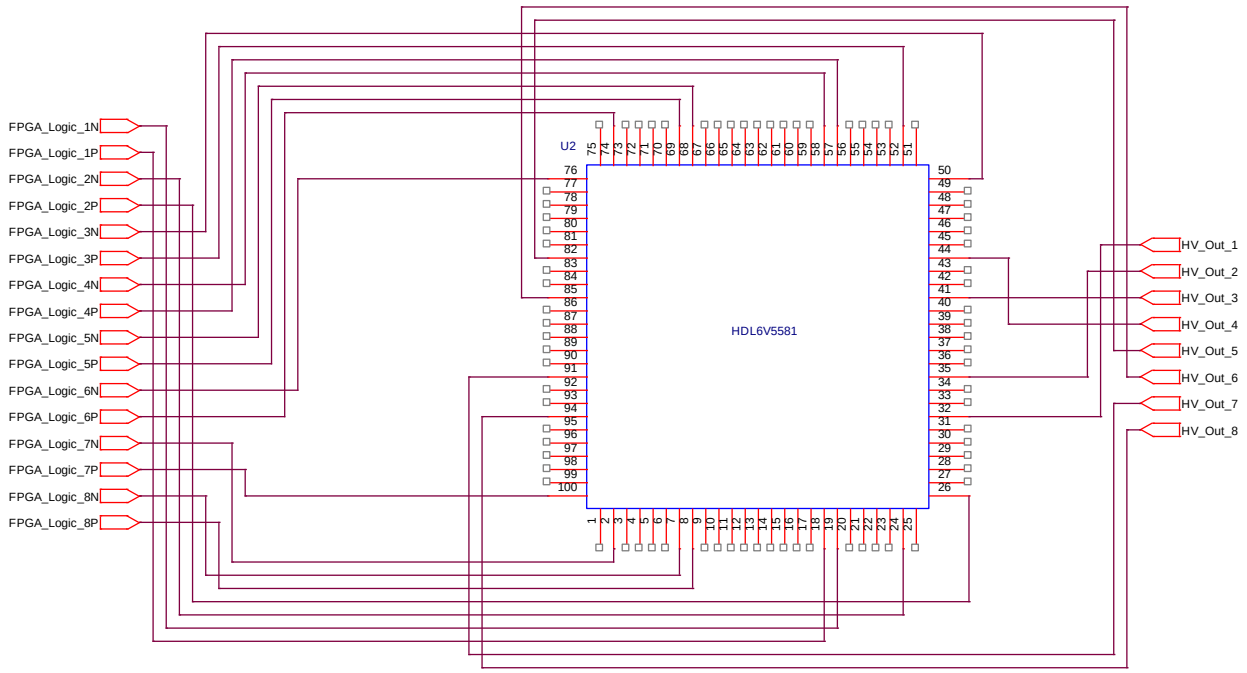


Figure 3 – HDL6V5581 Application Circuit

The application circuit follows the suggestions given in the HDL6V5581 datasheet. It should also be noted that the power interfaces of the device are not detailed in Figure 3. The power pins will follow the suggestions given in the HDL6V5581 datasheet regarding bypass capacitor placement and board layout.

The inputs to the HDL6V5581 will be provided by the XLINX FPGA evaluation board. A table illustrating the input pins and interface with other devices is given below:

Input Pin Name:	Logical Characteristics:	Incoming Signal from:
Pin#	If this pin receives a "high" signal, the output is pulled down to the VPP_ voltage	FGPA HPC connector
Nin#	If this pin receives a "high" signal, then the output is pulled up to the VNN_ voltage	FPGA HPC connector
EN	Enables all of the channels if driven low	Will be enabled by the computer interface

Note: The inputs to the HDL6V5581 will be logical CMOS signals ranging from 0 to 5V. The XLINX FPGA board is capable of signaling speeds of up to 7 GHZ, which will be adequate for producing small duty-cycle (~10%) 3 MHz signals.

Next, a brief description of the operation of the HDL6V5581 will be given in order to understand how the device will operate. The HDL6V5581 will drive two different power MOSFETS in order to perform high voltage switching. The equivalent circuit for one channel of the device is shown below in Figure 4.

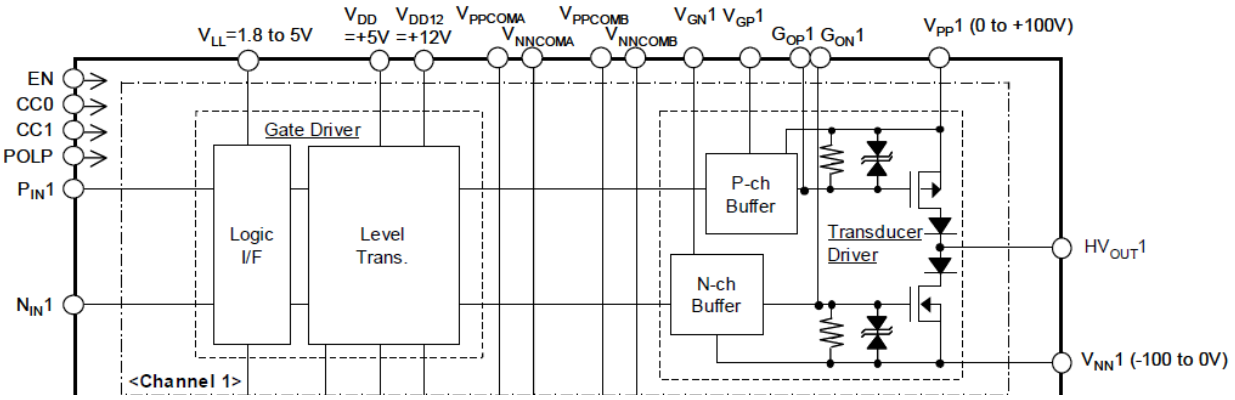


Figure 4 - Equivalent Circuit for High Voltage Switching

In Figure 4, the MOSFET gates are driven by specialized circuitry in order to "turn on" the devices. The gate-driver circuitry is labeled as "Level Trans." in the Figure above. When "high" logical signals are applied to the Ninx pins, the N-Channel MOSFET will current from the 100V source and pull the output voltage to 100V. When "high" logical signals are applied to the Pinx pins, the P-channel MOSFET will conduct and pull the output voltage down to -100V. Essentially, the HDL6V5581 allows for two individual logic control signals to control power MOSFETs that switch high voltages into the signal path.

The outputs of the application circuit shown in Figure 3 are +/-100V amplitude pulses that will be sent to the ultrasonic transducer. Each output of the pulser circuit can source/sink up to 2.5A, which indicates that the entire ultrasound transmitter will draw up to 80A during a transmission. The interface between the pulser and the ultrasound probe will be described in more detail later in this report.

Output Multiplexing

In order to reduce the amount of hardware needed to drive a 128-element transducer, the outputs of the transmitter can be multiplexed to the ultrasound interface. Such multiplexing allows for a small amount of circuit outputs to connect to the large number of ultrasound elements. Utilizing this concept, this ultrasound system design will only consist of a 32-channel transmitter/receiver circuit that will be switched to connect to all of the 128 transducer elements. Figure 5 illustrates this concept in relation to the other hardware that has been introduced in this document.

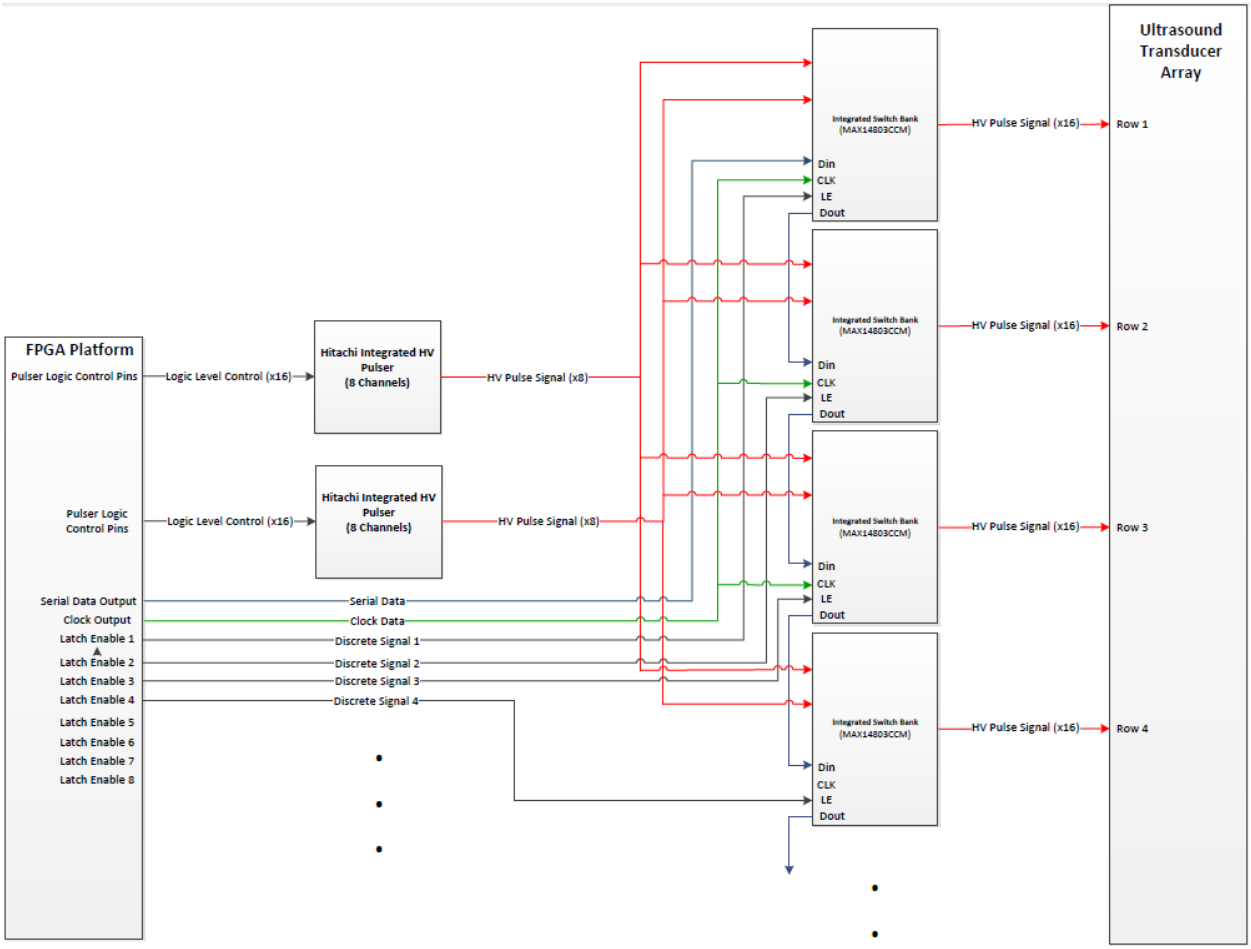


Figure 5 – Ultrasound Output Multiplexing

While Figure 5 details numerous interfaces between devices, the general operation of the circuit can be understood by examining it carefully. The FPGA control of the Hitachi Pulsers, which was explained thoroughly proceeding this section, is shown at the left-most side of the diagram. Moving right in Figure 5, the outputs of the Hitachi pulser are shown to be connected to "Integrated Switch Bank" blocks. Each of the "Integrated Switch Bank" blocks consists of 16 serial-programmable SPST switches that connect directly to the ultrasound transducer elements. Therefore, it is possible to connect four eight-output Hitachi pulsers (32 outputs total) to an array of eight 16-channel Integrated switch banks (128 outputs total) that connect to 128 ultrasound transducer elements. The outputs of the pulsers can then simply be multiplexed to the ultrasound transducer in any order by enabling which switches are "on" via a serial interface.

Another aspect of Figure 5 to note is that only one serial interface is used to program all of the Integrated Switch Banks. The MAX14803 Integrated Switch Bank has both a serial input and serial data output, and the serial data output can be sent to another device input. Therefore, the serial interfaces for the devices can be daisy-chained together to allow for one interface to program all of the switch banks. In order to control which device(s) are being programmed, "Latch Enable" pins are present on each device that control whether to hold a previous set of values or load new values.

Specifications for the MAX 14803 Integrated Switch Bank are listed below:

Parameter:	**MAX14803 Specifications:**	**Desired Value:**
Number of Available Switches	16 integrated SPST switches	Desired: An integrated array of 16-32 switches
Maximum Voltage/Current Limits	Up to +100V/-100V Voltage on each channel. Up to 3A of current on each channel	Handles up to +100V/-100V Handles up to 2.5A of current per channel.
Serial Interface	Each device features a 20MHz serial interface that operates at 5V. Serial interfaces between devices can be daisy-chained for simplified control. "Latch Enable" pins control whether the devices retains its currently programmed state or loads a new state in.	The device will feature an interface that will allow for each switch to be controlled individually.

From the table above, it is evident that the Integrated Switch Bank will be a suitable component for the design.

A schematic incorporating all of the components discussed in this section is shown below in Figure 6

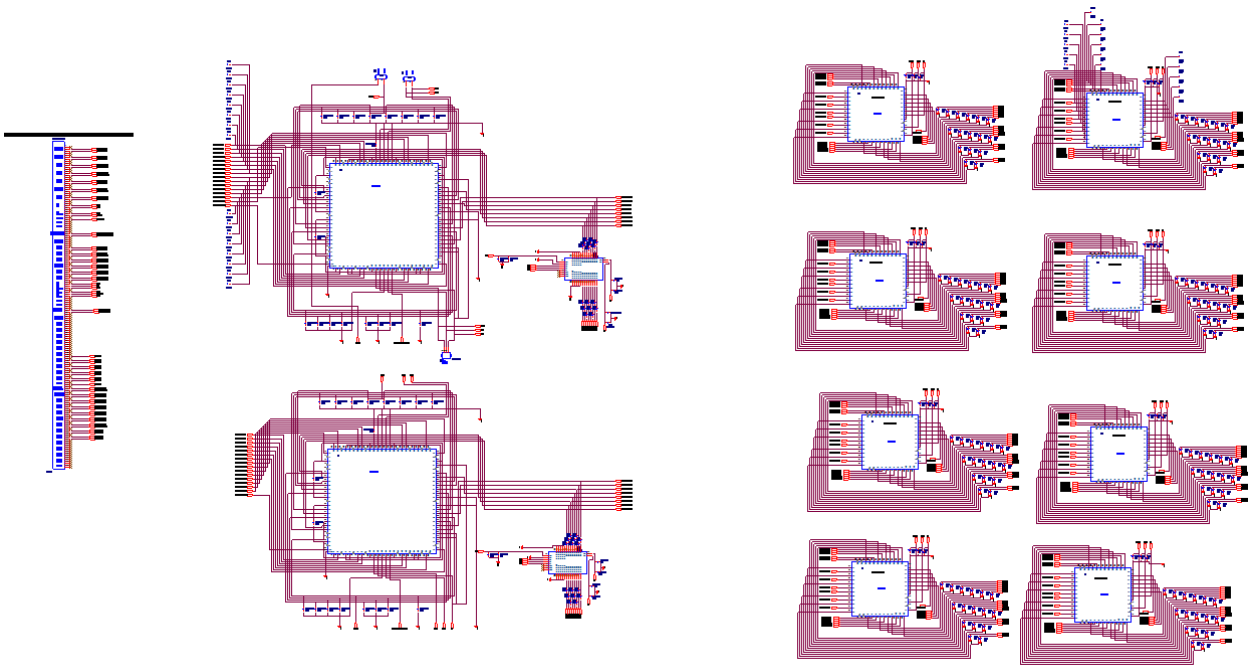


Figure 6 - Complete Ultrasound Transmitter Schematic

Power Electronics Design

Two separate power sources will be used to power the system's device circuitry. The main power supply will be 12V; while there will be another power supply of 100V that will be used for generating high voltage magnitudes for the ultrasound pulser IC. There are a total of 9 different voltage levels that will need to be regulated; +100V, -100V, +12V, +10V, -10V, +5V, -5V, +3.3V, +1.8V. The design will consist of a buck converter, positive and negative linear regulators, and an inverting regulator.

A flow chart below depicts how the voltages will be regulated.

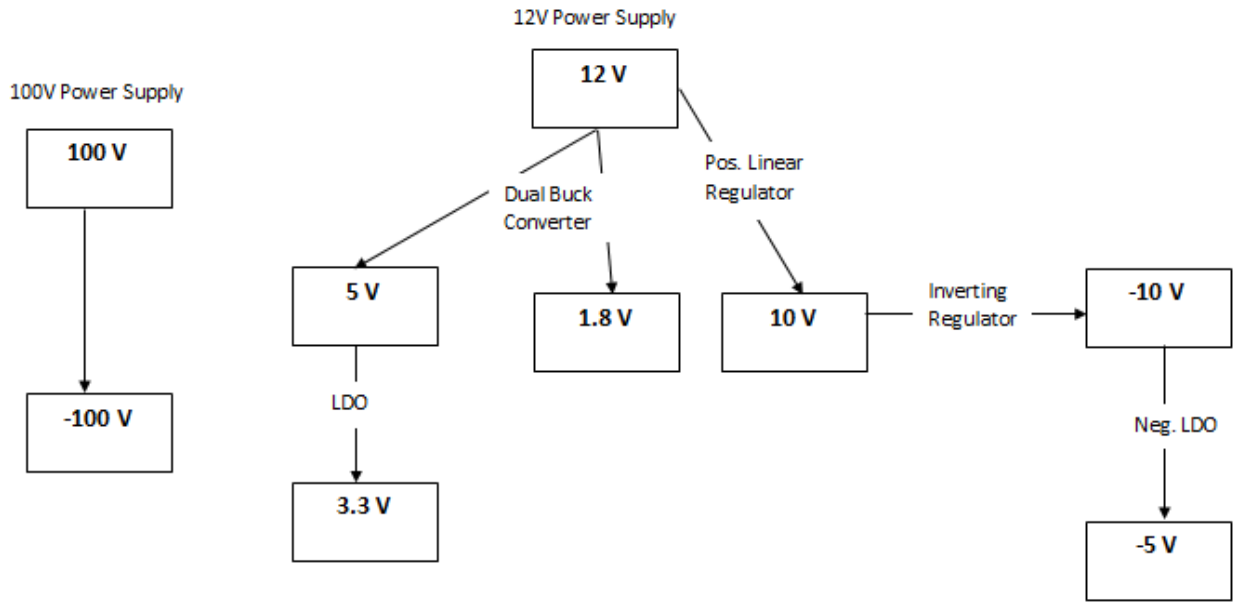


Figure 7: Power Flow Diagram

For the different power electronic components we chose Texas Instrument power regulating ICs. The components that were used are listed below:

- TPS54286 – Dual Buck Converter
- TPS7A4901 – Positive Linear Regulator
- TL497A – Inverting Regulator
- TPS7A3001 – Negative Linear Regulator
- TPS76933 – 3.3V Linear Regulator

100V Power Supply

The 100V power supply will connect with the Hitachi HV pulser. It will provide power for the positive and negative high voltage supply needed to amplify the incoming signals.

TPS54286 - Dual Buck Converter

The dual buck converter is used to regulate the 12V power supply to 5V and 1.8V. Texas Instruments provided schematics of external circuitry and the proper equations to select the external component values. A design procedure and external circuit set up was provided in the Texas Instruments datasheet. The procedure on selecting the external component values is followed by the schematic that is shown below.

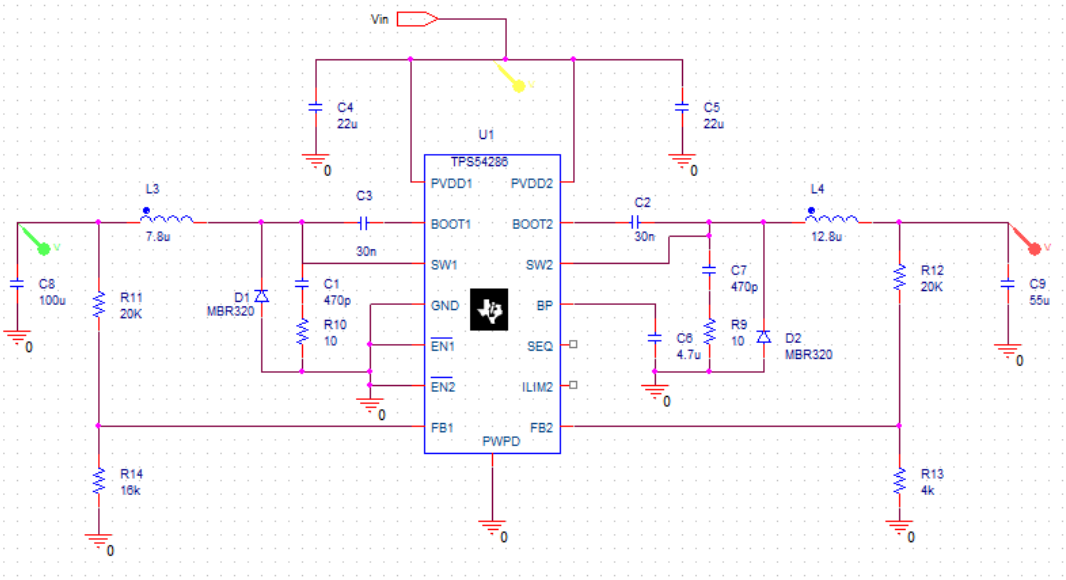


Figure 8: Dual Buck Converter Schematic

The minimum duty cycles of the circuit are described as:

$$D_{min} \approx \frac{V_{OUT} + V_{FD}}{V_{IN(max)} + V_{FD}}$$

The forward drop voltage, V_{FD}, for a schottky rectifier diode was assumed as 0.5V. Using the 5V and 1.8V output the minimum duty cycles were:

$$D_{5V,min} = \frac{5V + 0.5V}{12V + 0.5V} = 44\%$$

$$D_{1.8V,min} = \frac{1.8V + 0.5V}{12V + 0.5V} = 18.4\%$$

The inductor selection was governed by:

$$L_{min} \approx \frac{V_{IN(max)} - V_{OUT}}{I_{LRIP(max)}} \times D_{min} \times \frac{1}{f_{SW}}$$

The TSP54286 has a fixed switching frequency of *600kHz*. The maximum inductor ripple current is 600mA.

$$L_{5V,min} = \frac{12V - 5V}{600mA} \times 44\% \times \frac{1}{600kHz} = 12.8\mu H$$

$$L_{1.8V,min} = \frac{12V - 1.8V}{600mA} \times 44\% \times \frac{1}{600kHz} = 7.8\mu H$$

A schottky diode is selected as a rectifier diode for the low forward voltage drop. In the selection of the schottky diode the breakdown voltage we found the minimum voltage breakdown value.

$$V_{(BR)R(min)} \geq 1.2 \times V_{IN}$$

$$V_{BR,min} = 1.2 \times 12 = 14.4V$$

The diode must have a reverse breakdown voltage greater than 14.4V. A 20V device was used. The diode part number is MBRS320.

The output capacitor selection used the following equation:

$$C_{OUT} = \frac{1}{4 \times \pi^2 \times (f_{RES})^2 \times L}$$

The resonance frequency, f_{RES}, is about $6kHz$ for a ripple current of 600mA. The C_{OUT} values were calculated as follows:

$$C_{5V,OUT} = \frac{1}{4 \times \pi^2 \times 6000Hz^2 \times 12.8\mu H} = 55\mu F$$

$$C_{1.8V,OUT} = \frac{1}{4 \times \pi^2 \times 6000Hz^2 \times 78\mu H} = 90\mu F \rightarrow 100\mu F$$

The other capacitor values (i.e. the input, boot strap and BP) were given in the design example. This led us to selecting C4=C5=22µF, C2=C3=30nF, and C6=4.7µF.

The voltage setting feedback divider resistors, from V_{OUT} to FB, should range between 10kΩ and 50kΩ. A value of 20 kΩ was used for the R11 and R12 resistors. The selection of the R13 and R14 resistors used the following equations:

$$R13 = \frac{V_{FB} \times R12}{V_{OUT1} - V_{FB}}$$

$$R14 = \frac{V_{FB} \times R11}{V_{OUT2} - V_{FB}}$$

The forward bias voltage, V_{FB}, is given as 0.8V. Using those equations R13=3.83kΩ and R14=16kΩ. It is suggested that we add a RC snubber on the switch nodes to reduce the ringing. These values were given in the document as C1=C7=470pF and R9=R10=10Ω.

The designed circuit, along with the model of the TPS54286 IC was simulated in PSPICE. The transient analysis results are show below.

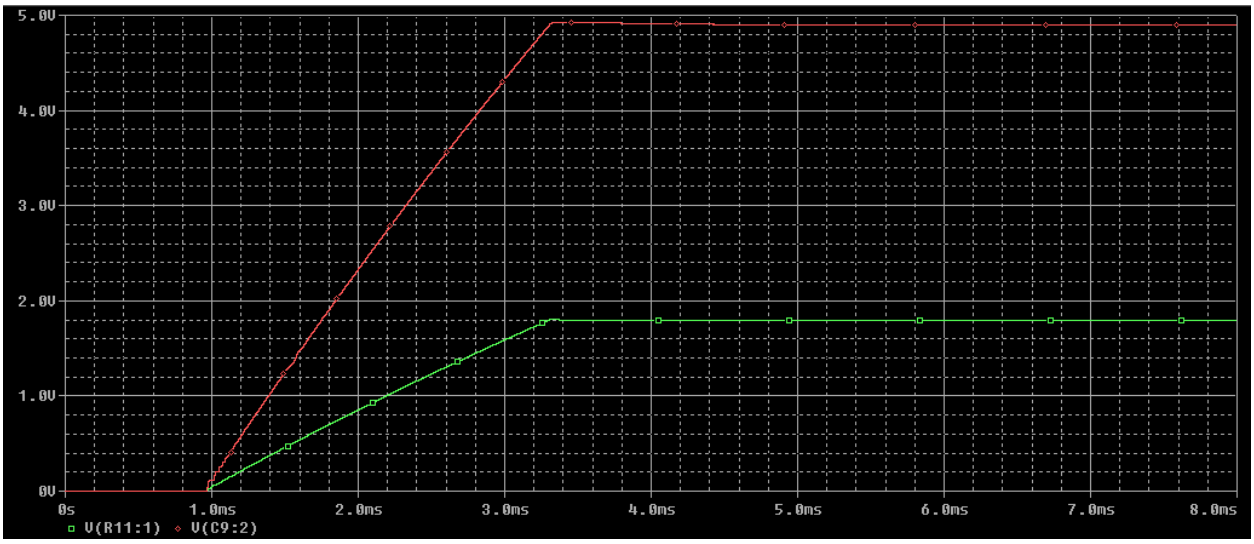


Figure 9: TPS54286 Transient Analysis Result

TPS7A4901 – Positive Linear Regulator

The positive linear regulator will be used to convert the 12V power supply voltage to 10V. Texas Instruments provided schematics of external circuitry and the proper equations to select the external component values. A design procedure and external circuit set up was provided in the Texas Instruments datasheet. The procedure on selecting the external component values is followed by the schematic that is shown below.

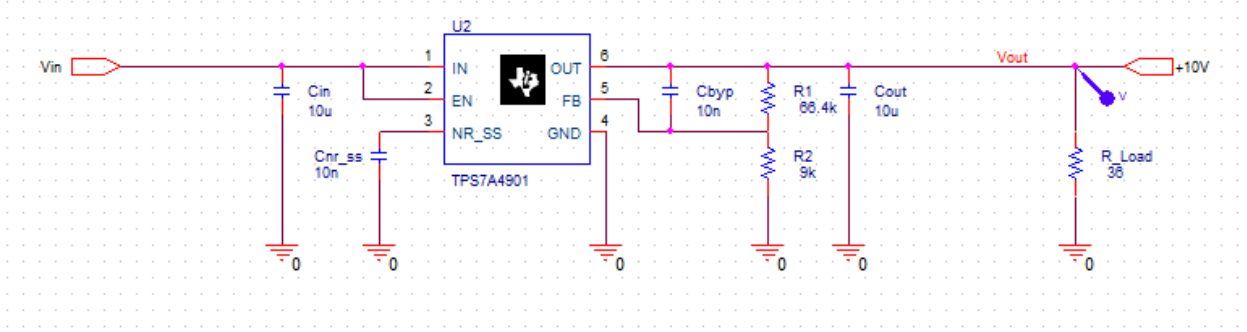


Figure 10: Positive Linear Regulator Schematic

The output voltage and the voltage divider equations were provided as:

$$R_1 = R_2\left(\frac{V_{OUT}}{V_{REF}} - 1\right), \quad \text{where } \frac{V_{OUT}}{R_1 + R_2} \geq 5\mu A$$

V_{REF} is the internal reference voltage and it is 1.194V. Selecting a R_2 resistance of 9kΩ yields a R_1 resistance of 66.4kΩ.

In selection of the input and output capacitors, we chose the values that Texas Instruments suggested in the datasheet. The noise and bypass capacitors are not needed, but they are recommended in the datasheet to minimize noise and maximize AC performance.

The designed circuit of the TPS7A4901 was simulated in PSPICE. The transient results are shown below.

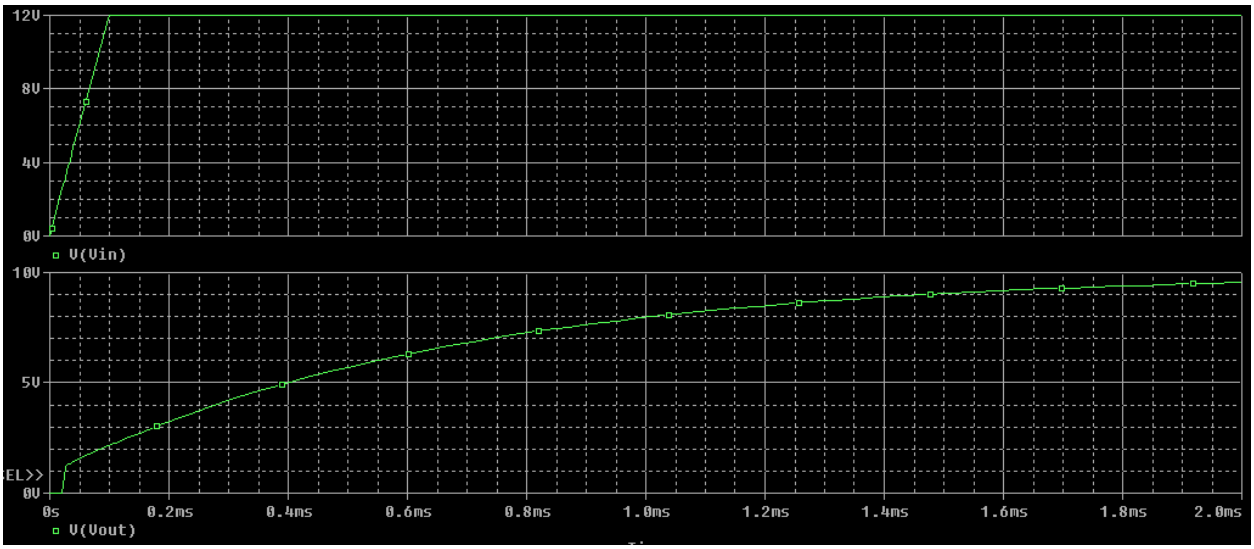


Figure 11: TPS7A4901 Transient Analysis Result

TL497A – Inverting Regulator

The inverting regulator will be used to convert 10V to -10V. Texas Instruments provided schematics of external circuitry and the proper equations to select the external component values. A design procedure and external circuit set up was provided in the Texas Instruments datasheet. The procedure on selecting the external component values is followed by the schematic that is shown below.

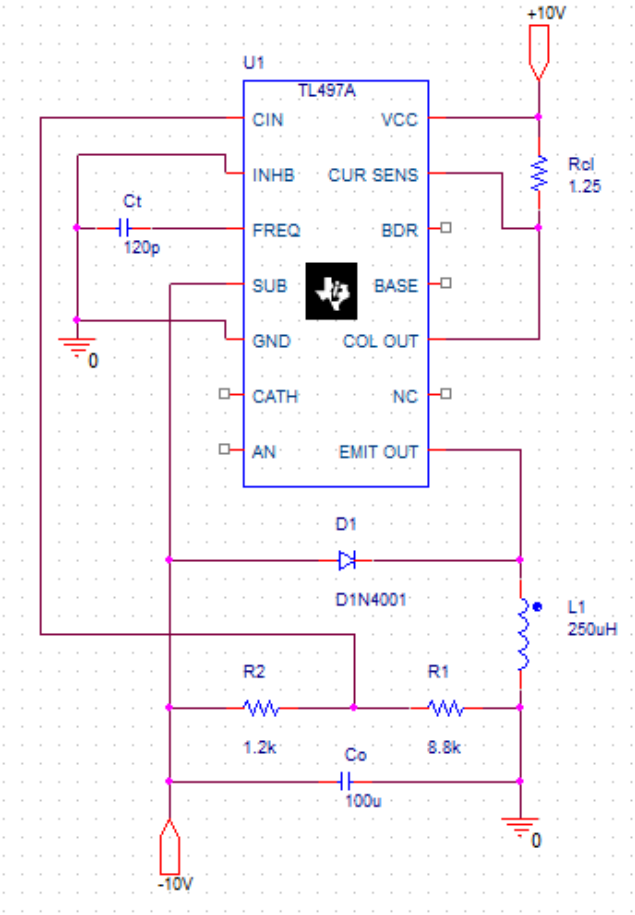


Figure 12: Inverting Regulator Schematic

The following equations were provided from the Texas Instruments datasheet. These equations were used in the design of the external circuit.

$$I_{(PK)} = 2\,I_O \max\left[1 + \frac{|V_O|}{V_I}\right]$$

$$L\,(\mu H) = \frac{V_I}{I_{(PK)}} t_{on}(\mu s)$$

$$C_T(pF) \approx 12\,t_{on}(\mu s)$$

$$R1 = \left(|V_O| - 1.2\,V\right) k\Omega$$

$$R_{CL} = \frac{0.5\,V}{I_{(PK)}}$$

$$C_O\,(\mu F) \approx t_{on}(\mu s) \frac{\left[\frac{V_I}{|V_O|} I_{(PK)} + I_O\right]}{V_{ripple}\,(PK)}$$

There were suggested values in the datasheet that were used in the design of the circuit. The suggested values were I_o=100mA, $V_{RIPPLE(PK)}$=50mV, R_2= 1.2kΩ, V_I=10V, V_O=-10V, and t_{ON}=10µs. Using these values yielded $I_{(PK)}$=0.4A, L=250µH, C_T=120pF, R1=8.8kΩ, R_{CL}=1.25Ω, and C_O=100µF.

TPS7A3001 – Negative Linear Regulator

The negative linear regulator will be used to convert the -10V to -5V. Texas Instruments provided schematics of external circuitry and the proper equations to select the external component values. A design procedure and external circuit set up was provided in the Texas Instruments datasheet. The procedure on selecting the external component values is followed by the schematic that is shown below.

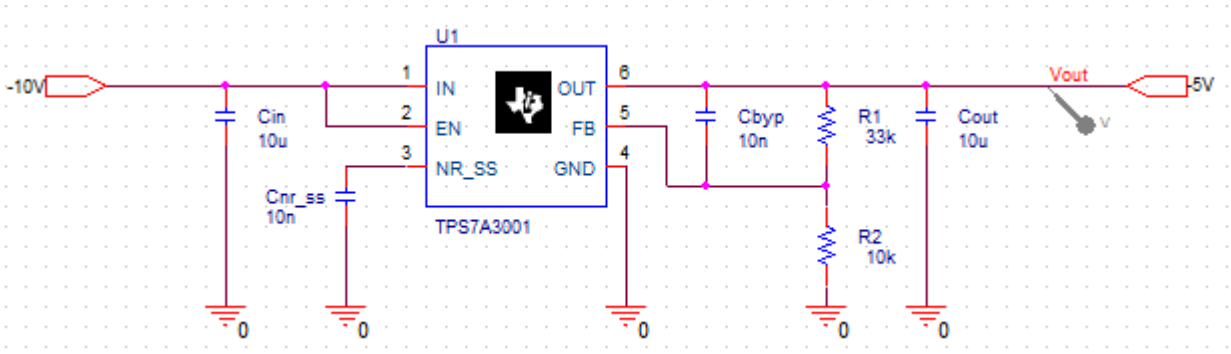


Figure 13: Negative Linear Regulator Schematic

The negative linear regulator used the same equations as the positive linear regulator. The voltage equations provided in the Texas Instruments datasheet are shown below.

$$R_1 = R_2\left(\frac{V_{OUT}}{V_{REF}} - 1\right), \quad \text{where} \quad \frac{V_{OUT}}{R_1 + R_2} \geq 5\mu A$$

V_{REF} is the internal reference voltage, and it is -1.184V. Selecting a R_2 resistance of 10kΩ yields a R_1 resistance of 33kΩ.

The designed circuit of the TPS7A3001 was simulated in PSPICE. The transient results are shown below.

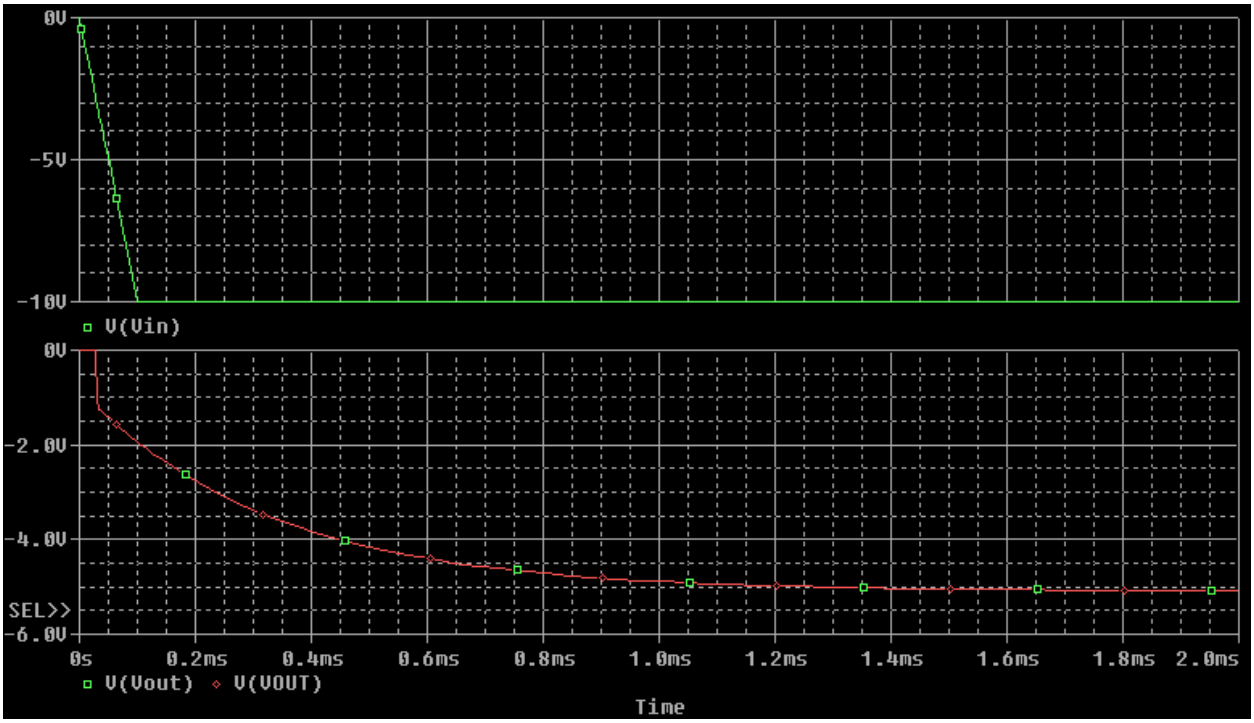


Figure 14: TPS7A3001 Transient Analysis Result

TPS76933 – 3.3V Linear Regulator

The 3.3V linear regulator will be used to convert 5V to 3.3V. There was no design procedure for this IC, since it is a fixed output regulator. The only external circuitry used was one input capacitor and one output capacitor. Texas Instruments datasheet suggested that the input capacitor be 1µF and the output capacitor be 4.7µF. The schematic is shown below.

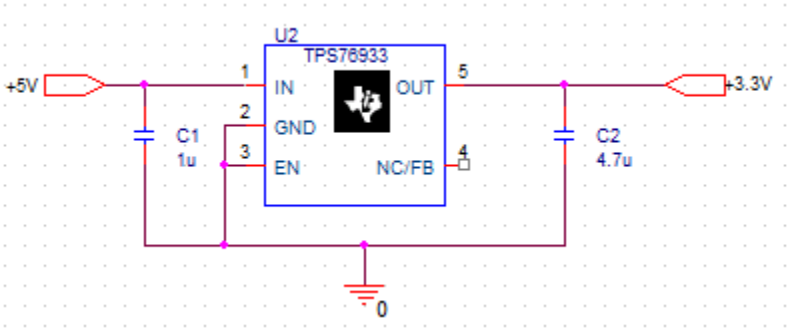


Figure 15: 3.3V Linear Regulator

Ultrasound PCB Design & Layout

Overview

There are three printed circuit boards (PCB) that completes the ultrasound imaging circuit. The sections that the PCB layout was divided into are the ultrasound imaging architecture, power electronics, and a mezzanine

connector. There is also a FPGA PCB that produces the signal generation for the system. The purpose of mezzanine connector is to interface the FPGA board with the main ultrasound imaging board.

PCB layouts were created in Allegro PCB Editor. Using PCB Editor allowed for the PCB Layout to be created with great detail and precision. PCB Editor is used in conjunction with OrCAD Capture; the PSPICE program that was used for creating the system schematics. Creating the schematics in Capture allowed for the design to be imported in PCB Editor where the designer would create the layout for the PCB.

PCB Design

In the PCB Design section a detailed description of the design process will be covered. Topics ranging from the board architecture to physical testing and implementation are discussed. A library of components was not provided for designing the PCB layout. Therefore a majority of schematic symbols for the ICs were created manually. All of the component footprints and padstacks, except for the Samtec connectors, were created manually. Once all of the footprints and padstacks were created and assigned to their components the PCB layout process was then conducted.

Ultrasound Imaging Board

The ultrasound imaging board (Figure 16) was designed to be a 12" x 12" board that consisted of 6 different copper layers. The reason for the size of this board was to provide adequate surface space for placing all of the components and room for the copper traces. The board has 5 layers for routing and a ground plane layer. The 5 routing layers gives the traces enough room to be spaced properly and to allow for all of the traces to correctly start and terminate at the correct pin.

Regarding the physical set up, similar components were placed near each other in order to keep a uniform design on the board. Every integrated circuit and external circuitry associated with the IC had their own "room" on the PCB board. Included in the room were the IC and the external circuit components. Creating rooms organized the board so specific components could be found easier along with reducing trace lengths during routing. Having a uniform design reduces the difficulty of the soldering process and debugging.

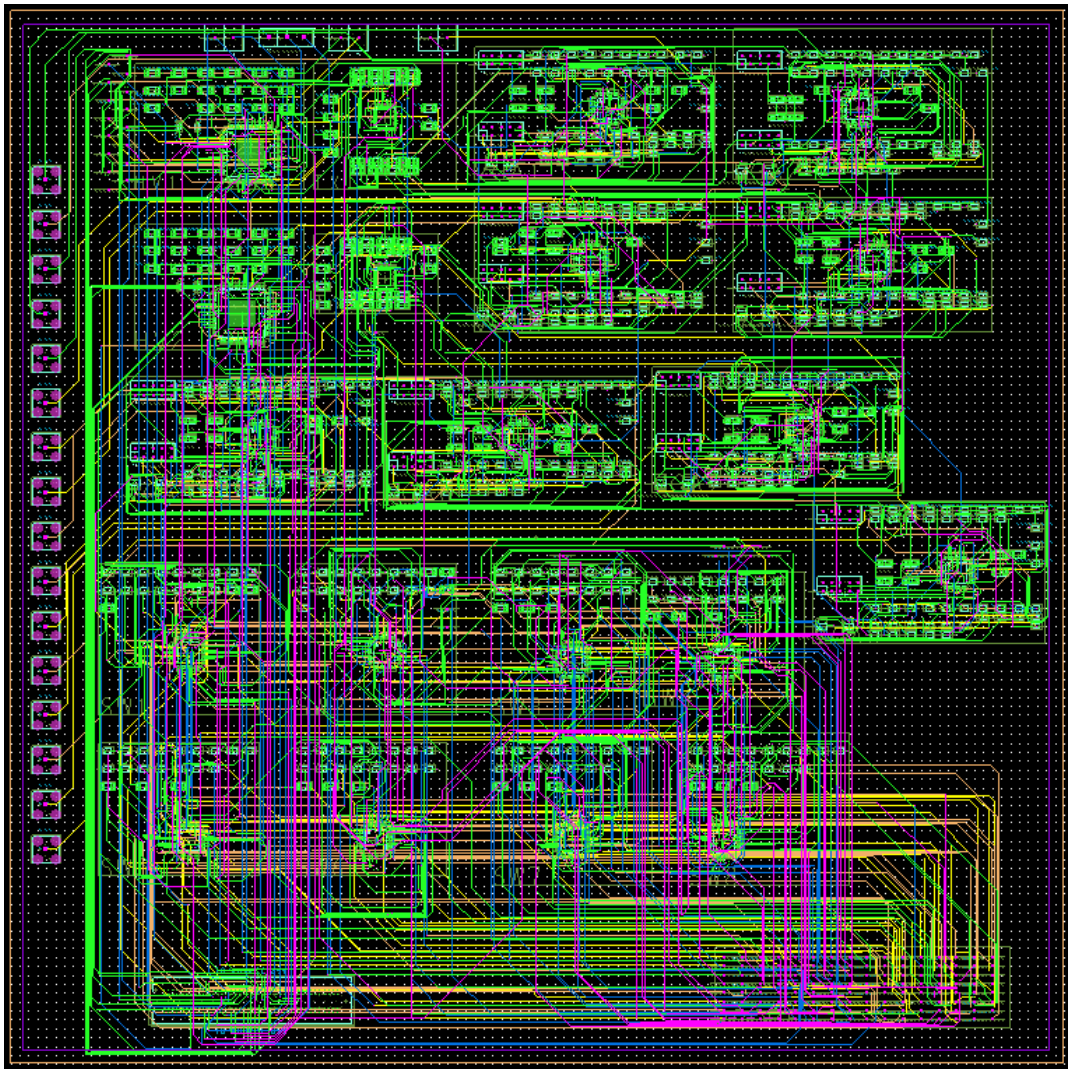


Figure 16: Ultrasound System Layout

Power Electronics Board

The power electronics board (Figure 17) was created separately to reduce the size of the main board. This board is significantly smaller being 2 layers and having the dimensions of 5" x 4". The power electronics board consists of all the power electronic ICs that regulate the voltage for the system. The outputs on the power electronic board are terminal blocks that will allow for hardwiring the power sources.

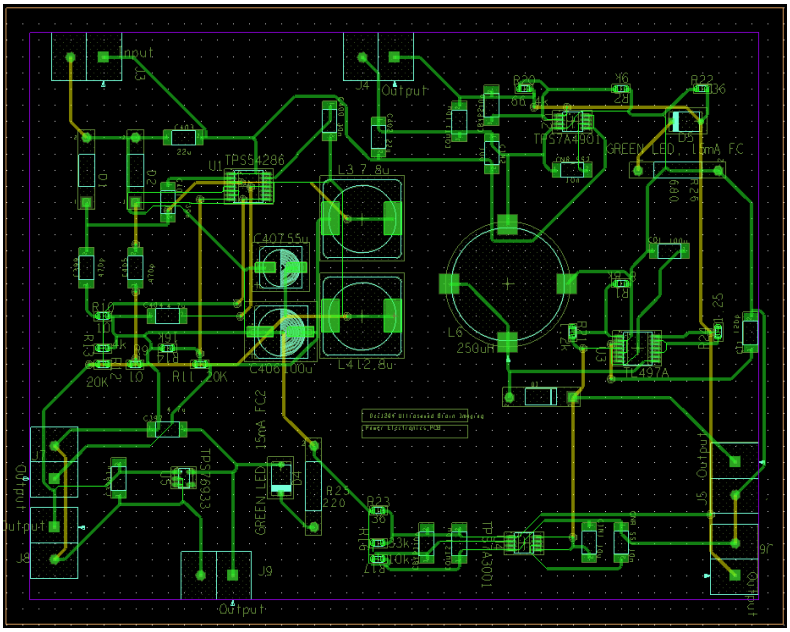


Figure 17: Power Electronics Layout

Footprints

PCB footprints are files that determine the location, outline of package, and geometry of the pads on the various components on the printed board. Pads are areas where the pins are soldered to the board. Footprints are required for the ICs, capacitors, resistors, inductors, amplifiers, terminal blocks, and through-hole test points. These files are used to lay out the circuit in PCB Editor. Figure 18 displays the footprint file for the switch banks used.

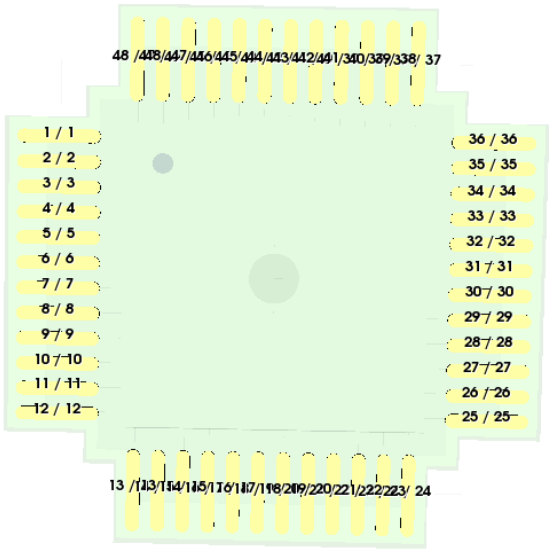


Figure 18: Switch Bank Footprint

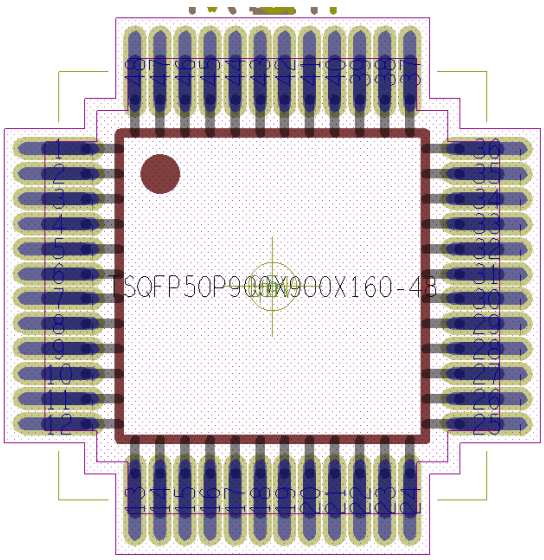


Figure 19: Switch Bank Footprint & Padstack

Padstacks

Padstacks are files that contain information regarding the pad size and shape, drill size, drill display figure, and soldermask for the top and bottom layer of the board. Also, they determine how the inner layers are connected. Padstack files work in conjunction with the footprint files associating the pins to the proper pad. Padstacks are necessary for drill holes, vias, surface mount pins, through-hole components, and testing points. Figure 4 shows the switch bank footprint along with the padstack shapes and sizes.

To create the footprints and padstacks Footprint Maker 0.0.8.0 was used. This program offered a way to create footprints where the user defines the package type and dimensions. The datasheet of the components provided the packaging dimensions, which was used to create the footprints in Footprint Maker. An example of a Quad Flat Package, similar to the Hitachi HDL6V5581 pulser, is shown in Figure 20.

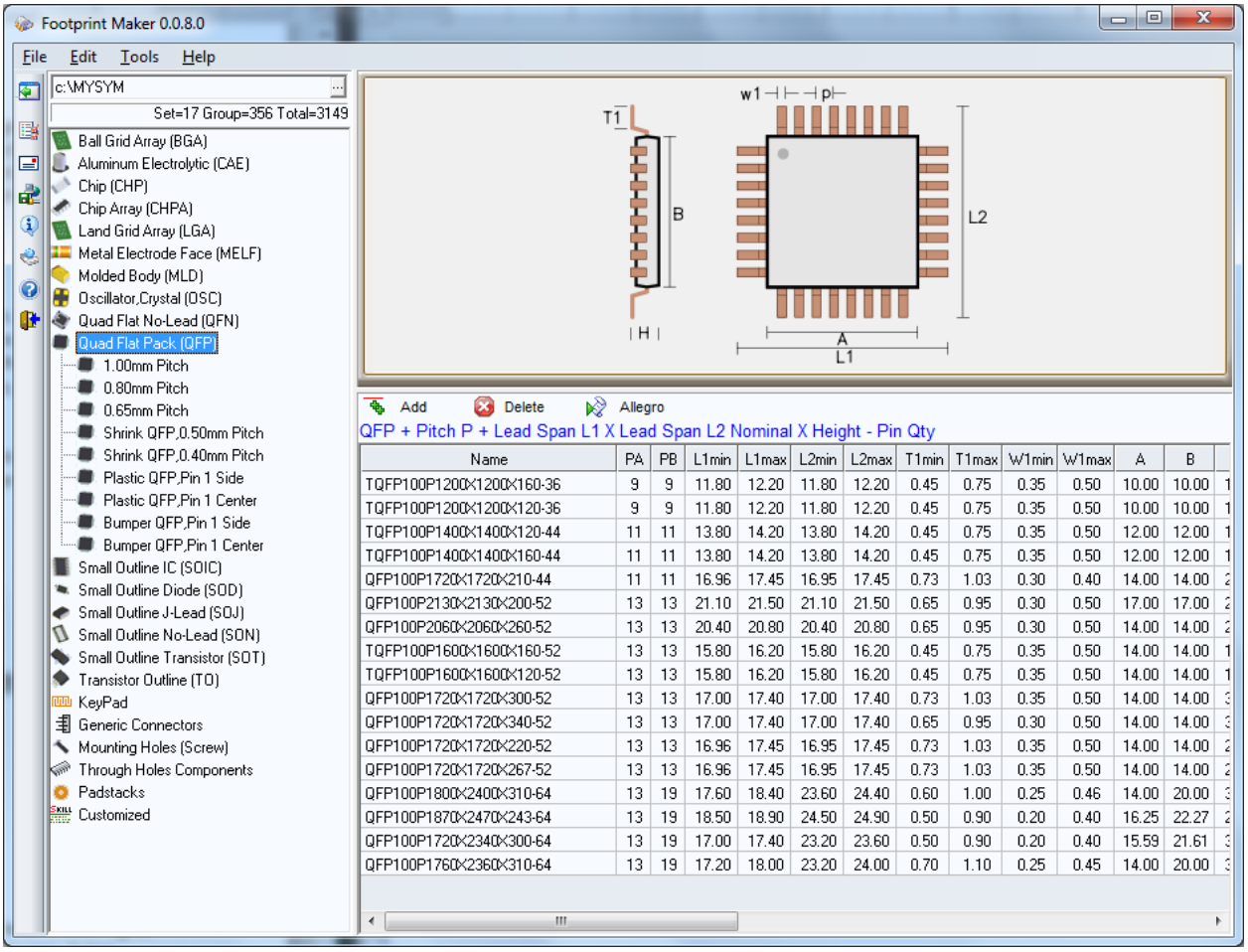


Figure 20: Footprint Maker

Routing

Routing a small two layer circuit can be trivial, but when it comes to routing a large, six layer circuit it can be a daunting task. PCB Editor has a built in auto route function that was used to route the PCB. Along with the built in function another program, OrCAD PCB Router, was used. PCB Router allowed for the setup of the routing to be defined. The routing parameters were defined by user preference, but governed by the

manufacturer. The manufacture guidelines determined the spacing of traces and vias, drill hole sizing, soldermask sizing, drill holes, and silkscreen line width.

Testing Points & Terminal Blocks

Testing points were implemented into the design to test and validate signal generation and manipulation. Terminal blocks were not only used as power sources, but as points where the voltage could be validated for the correct regulation.

The testing points are located at the inputs to the high voltage pulser and at the inputs and outputs of a switch bank. Having test points at these locations allowed for monitoring of the input, transmit, and receive signals.

DFM Check

Once the completed printed circuit board was exported as gerber files ready to be sent for manufacturing a FreeDFM (www.FreeDFM.com) check was conducted. Design for manufacturability check is used to verify that the design files are free of any errors that would cause a problem in the manufacturing process.

Mezzanine Connector Board

When looking at options to connect the FPGA board to the ultrasound imaging board it is a priority to ensure that the signals and connections can be tested. It is important to test the signal before entering the ultrasound imaging board to be able to isolate any problem. The design for the mezzanine connector board contains the following components to help test and send the signal.

- (2) Vita connectors that contain 4 rows of 40 pins
- (3) rows of 32 connecting header pins
- (2) LED status lights
- (2) resistors
- (1) transistor

The Vita connectors have enough pins to transmit all the signals from the FPGA board to the ultrasound imaging board. The signal leaves the FPGA through the mating Vita connector and then goes to the connecting board. Selected signals are then tested before going to the matching Vita connector on the other side of the board. There are also two LEDs on the board that show if the signal is being transmitted. After that the signal leaves the connector board and enters the ultrasound imaging board through a mating Vita connector. Below is the PCB layout of the board showing the three rows of pins that are used as test points for the signals. The left picture (Figure 21) shows the entire PCB layout of the mezzanine connector. The right picture (Figure 21) contains only the components on the board.

Figure 21 - Layout of the Mezzanine Card

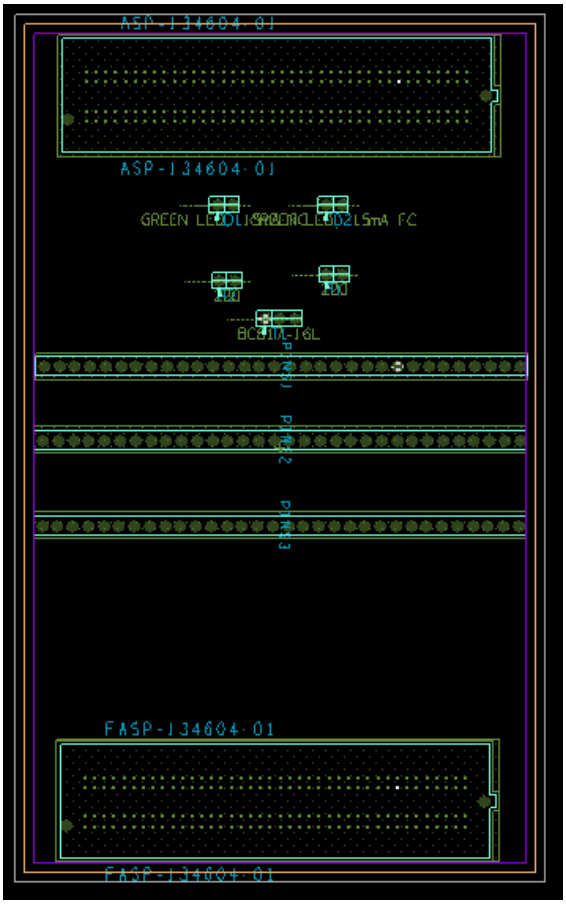


Figure 22 – Components on the Mezzanine Card

The dimensions of the board are 2.717" by 4.425". Even with the smaller sized board, all the wires that are needed can fit on a two layer board. Senior design groups get discounts on two layer boards that are smaller than 60 square inches. This falls into that category and helped save the team money. In Figure 21, the 3 rows of header pins will be used to test selected signals that are being transmitted to the ultrasound imaging board. The footprints for the Vita connectors were provided by Samtec, Inc. These footprints are the exact footprints for the connectors that were ordered. All the other footprints were created by the team by the process mentioned earlier. The Pspice schematic for the test circuit containing the LEDs is in Figure 23. If the mezzanine connector board is properly working than LED2 in Figure 21 will be on. If the signals are not being transmitted than LED1 will be on.

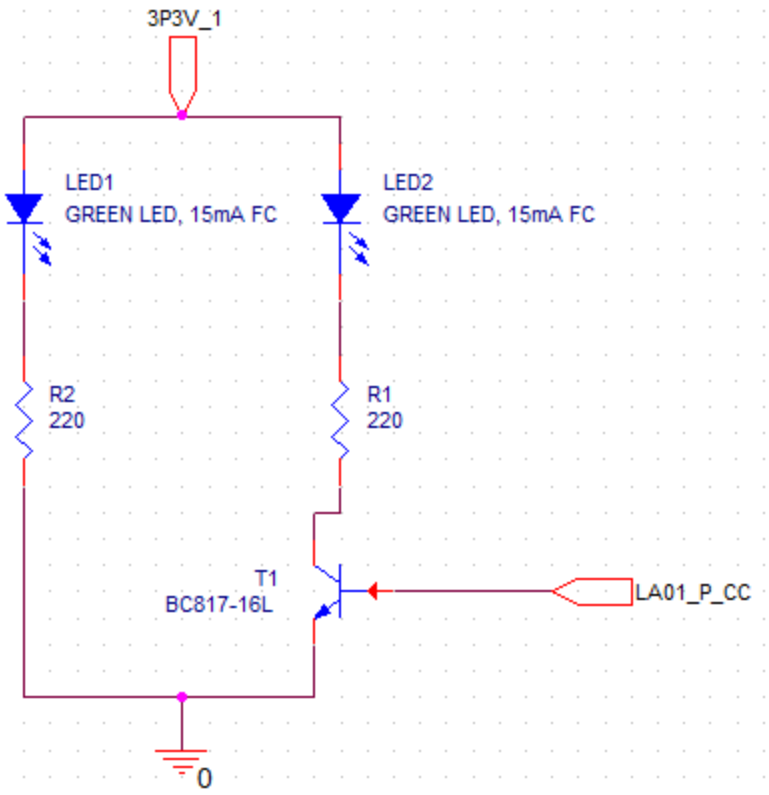


Figure 23 - LED Test Circuit on FPGA Mezzanine Card

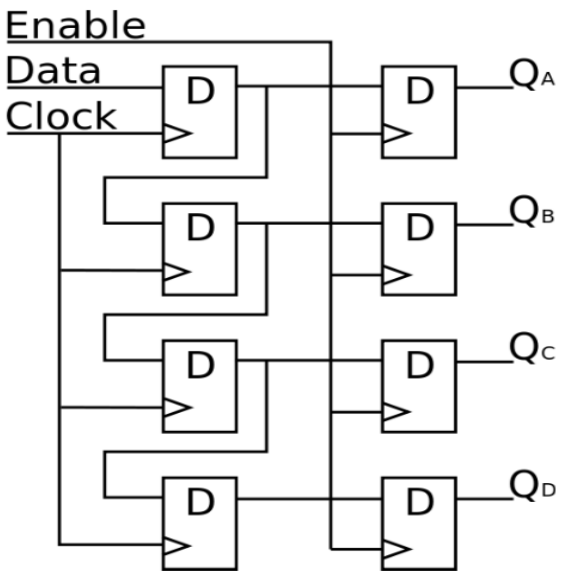
The mezzanine connector board is a crucial part of the design process, even though it is smaller and requires only a few components. Without the board the FPGA will be unable to send signals to the ultrasound imaging board. Also with the mezzanine connector board, tests can be performed to help narrow down problems with the circuitry.

Hardware Control Interface Design

The system requirements for the pulse-echo ultrasound system define a controllable channel phase ranging from 10 ns to 20 us and a controllable amplitude from 0-80V. In order to meet these demanding requirements, a state-machine was implemented on a Virtex-6 FPGA. The state-machine runs individual logical modules created to control each interface of the ultrasound transmitter. These logical modules include a serial interface to program the switch banks, a logic interface to control the pulser inputs, and a pulse-shaping algorithm to control the rate of signaling on the pulser input interface. An explanation of each module is given below.

Switch Bank Control Module

The purpose of this control module is to run a 20Mhz serial interface to the switch bank and program which switches are closed. The internal circuitry of each switch bank consists of a 16-bit shift register and 16 flip-flops connected to each flip-flop in the shift register. Figure 24 illustrates the digital interface to the switch bank:



Serial Data bits are passed through a 16-bit shift register

Once the desired switch configuration is set in the shift register, pulse the latch control to program

Figure 24 – Portion of Switch Bank Digital Circuitry

Serial data is clocked into the interface shown above through the data input wire, and each bit passes through the shift register on rising clock edges. Once the desired bit sequence has been clocked into the shift register, a latch-enable input must be toggled to load the contents of the shift register into the latches to program the switches. A signal diagram illustrating the programming of the switch bank through the shift register/latch interface is shown below in Figure 25.

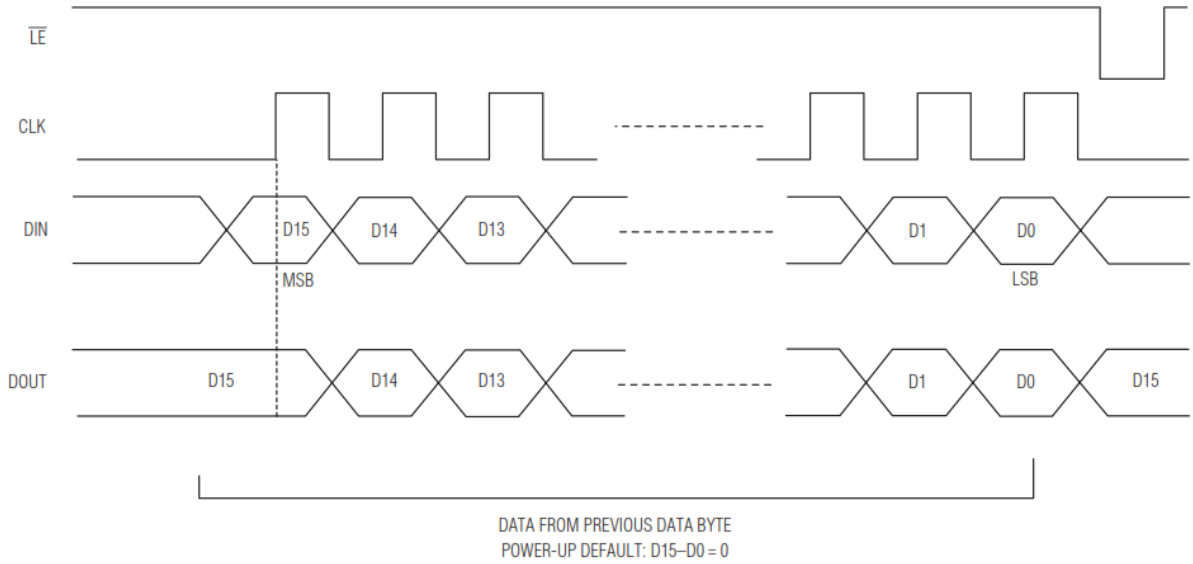


Figure 25 - Maxim 14803A Serial Interface Timing Diagram

In our application, a selected switch bank will be programmed so all switches are closed. In order to program all switches closed in a bank, 16 "ones" must be clocked into the shift register before the latch-enable signal is pusled low to load the contents of the shift register into the switch bank latches. Additionally, the Maxim integrated switch bank serial interface can be daisy-chained to other devices. Daisy-chaining the switch banks allows for one serial interface from the FPGA to control all eight switch banks utilized by the system.

The daisy-chained configuration of the switch bank serial interfaces simplifies the hardware implementation considerably. However, the trade-off is that the FPGA hardware must compensate for the propagation delay through the daisy-chained interface. If the last switch bank in the chain is to be programmed, data must be clocked through 112 flip-flops before reaching the last bank. The worst-case propagation delay due to the daisy-chained interface is approximately 6 us.

With the propagation delay through the interface analyzed, other aspects of the serial interface can be discussed. In order to ensure that the flip-flops in the serial interface start with a valid state when they are programmed, a clear signal can be toggled to load the latches with a logical zero. Data can be clocked into the switch bank shift register after the clear signal has been toggled. Summarizes the programming sequence needed to operate the switch bank serial interface.

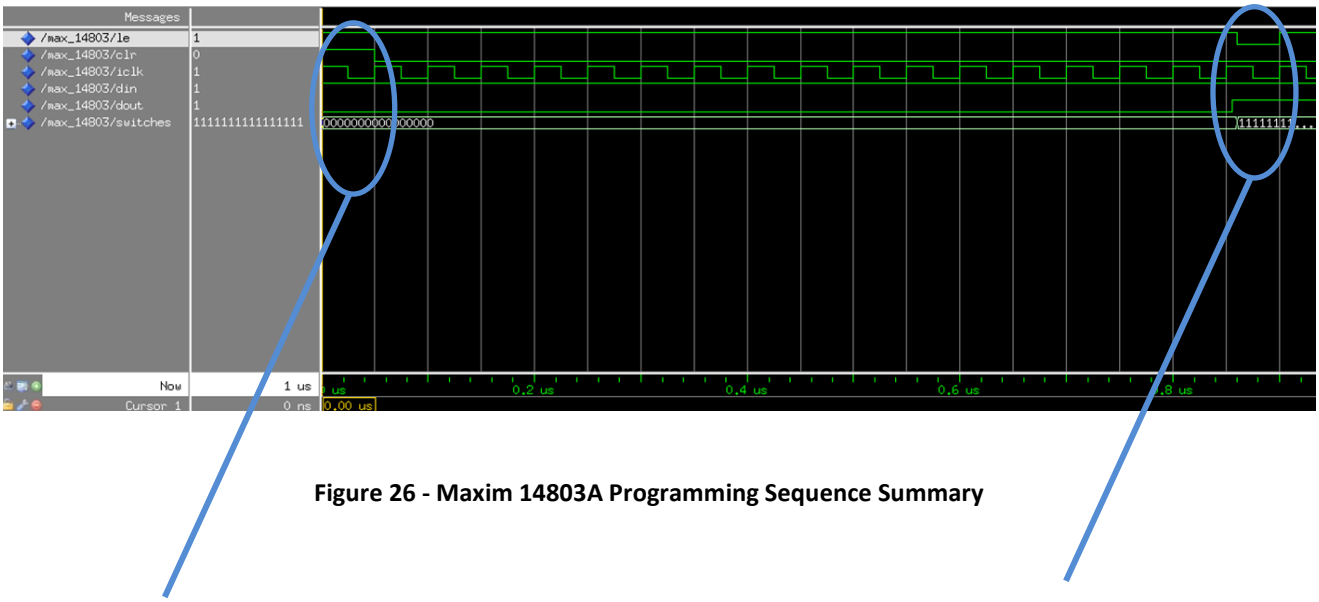


Figure 26 - Maxim 14803A Programming Sequence Summary

Initially toggle the "Clear" control to ensure the states of the latches in the device are storing logical zeros before programming

After all 16 values have been shifted into the MAX14803 register over the 20 MHz serial interface, toggle the LE control logic-low to load the contents of the shift register into the latch.

Considerations for the LE Control:

- There will be an appreciable propagation delay through the device that must be accounted for, the delay shown above (3ns) was obtained from the datasheet
- Therefore, the LE control must be toggled after 16 rising clock edges + propagation delay.
- LE pulse-width must be greater than 14ns

Pulser Control Interface

The logic interface to the Hitachi HDL6V5581 High-Voltage Pulser directly controls the eight outputs of the device. Utilizing this interface, the system requirements of a controllable amplitude from 0-80V and controllable phase between 10ns and 20 us can be realized. The interface between the FPGA and Hitachi pulser ICs can be observed in the system block diagram shown earlier in this report. Details regarding the implementation of the amplitude and phase control are given below.

The Xilinx ML605 evaluation board contains a Virtex-6 FPGA, interface circuitry, and multiple oscillators. In order to implement the pulse delay with a 10 ns resolution, a 200 MHz oscillator (5 ns clock period) on the ML605 board was used to clock the pulser module. Delays with the 200 MHz oscillator can be implemented in the FPGA by using a counter for each of the sixteen channels to count clock cycles. Once the desired delay for each channel has been achieved by counting clock cycles, a set of logic signals are sent to the Hitachi pulser to generate bipolar 80V pulses.

To illustrate the mapping between control signals and their applications, a truth table for the Hitachi HDL6V5581 digital circuitry is shown below in Table .

Table 4 - Hitachi HDL6V5581 Truth Table

Logic Input 1						HV MOSFET status				$HV_{OUT}xy$
EN	POLP	$P_{IN}x$	$N_{IN}x$	$P_{IN}y$	$N_{IN}y$	PMOSx	NMOSx	PMOSy	NMOSy	
0	0	1	0	0	0	**ON**	OFF	OFF	OFF	+HV1
0	0	0	1	0	0	OFF	**ON**	OFF	OFF	-HV1
0	0	0	0	1	1	OFF	OFF	**ON**	**ON**	GND
0	0	0	0	0	0	OFF	OFF	OFF	OFF	HiZ
1	X	X	X	X	X	OFF	OFF	OFF	OFF	HiZ

From the truth table shown in Table , it can be noted that logic signals applied to inputs labeled "Nin" will result in a negative high-voltage pulses and signals applied to inputs labeled "Pin" will result in positive high-voltage pulses.

Amplitude control for the pulses is accomplished through utilizing the network impedance of the ultrasound transducer. A pulse-width-modulated signal (PWM) can be applied to the ultrasound probe and the result will be a filtered waveform with an envelope corresponding to the PWM signal. A discussion of the exact implementation of the PWM signaling is discussed on is discussed in the next section.

Pulse-Shaping Module

Utilizing the fact that logic signals applied to the Hitachi pulser directly map to high-voltage pulses, the logic signals applied to the pulser can be controlled in order to shape the high-voltage output signal.. Instead of generating square waves with amplitudes corresponding to the high-voltage supply value, the network impedance of the ultrasound transducer can be used to filter the pulses and create a sinusoidal signal. Using the transducer to do this filtering results in an integrator circuit that can produce sinusoidal signals out of a

pulse-width-modulated signal. Figure 27 illustrates a simple model of the impedances that characterize the ultrasound transducer.

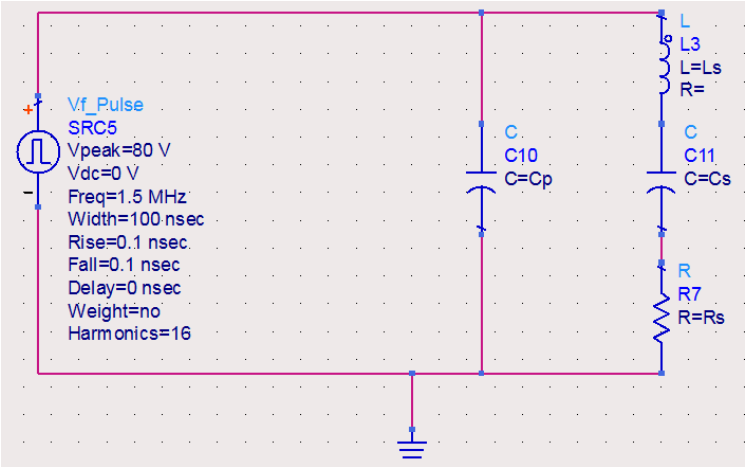


Figure 27 - Ultrasound Transducer Network

When the pulse generator (left side of the schematic in Figure 27) transmits into the network, it will encounter a reactive network that filters the pulse. The amount of filtering that occurs is dependent on the impedances that characterize the transducer. In order to determine these impedances, a network analyzer must be used to sweep an input frequency over a range near the operating frequency. Corresponding ultrasound probe impedances can be collected based off of the frequency sweep data. The company that designed and manufactured the ultrasound probe provided the Z-Sweep shown

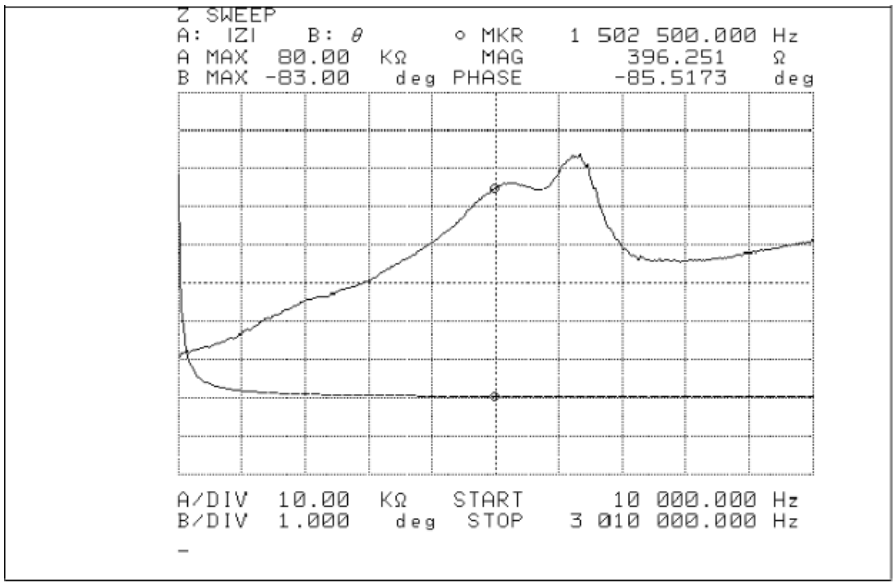


Figure 28 - Ultrasound Transducer Impedance vs. Frequency Sweep

Two curves are shown in Figure 28: a phase curve (with units of degrees) and a magnitude curve (with units of ohms). The combination of the values of these two curve at different frequency points gives a complex amplitude that corresponds to the total network impedance of the transducer. An attempt was made to

characterize the ultrasound transducer using the data shown in Figure 28, but the results (Figure 29 - Figure 31) did not match the given impedance information well. The source of this mismatch is assumed to be to poor magnitude resolution in Figure 28, and future groups will have to make more accurate measurements before proceeding with calculations.

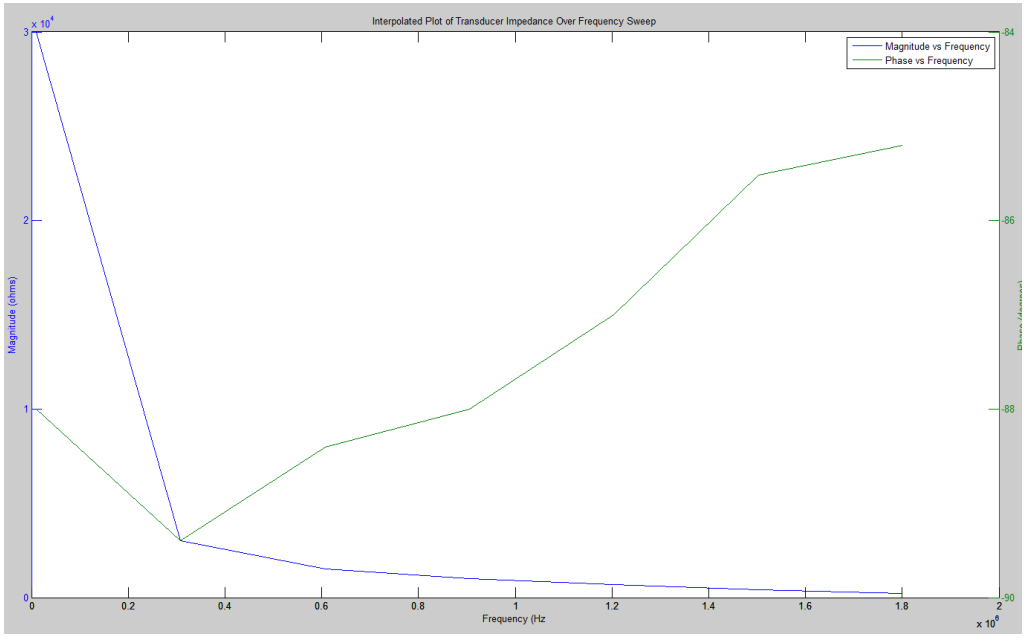


Figure 29 - Given Ultrasound Probe Impedance vs. Frequency Sweep Plotted in MATLAB

A MATLAB script was written to take a function handle representing the equation for the equivalent series impedance of the transducer and fit the function handle to a set of given data shown in Figure 29.

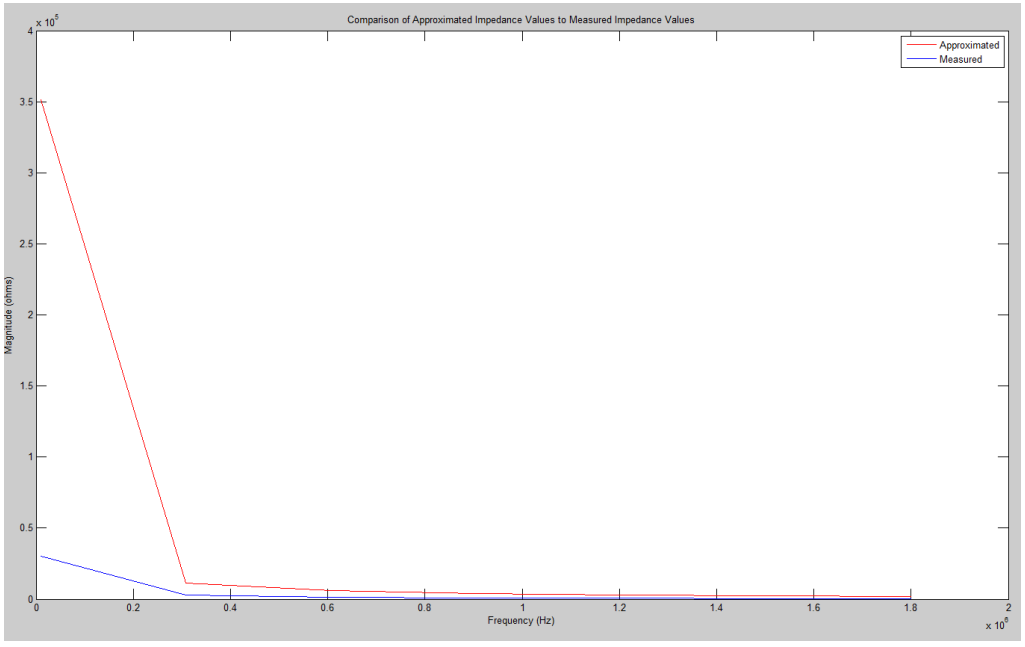


Figure 30 - Plot of Computed Network Magnitude (Red) vs. Given Network Impedance (Blue)

The result of the magnitude fit is shown in Figure 29.

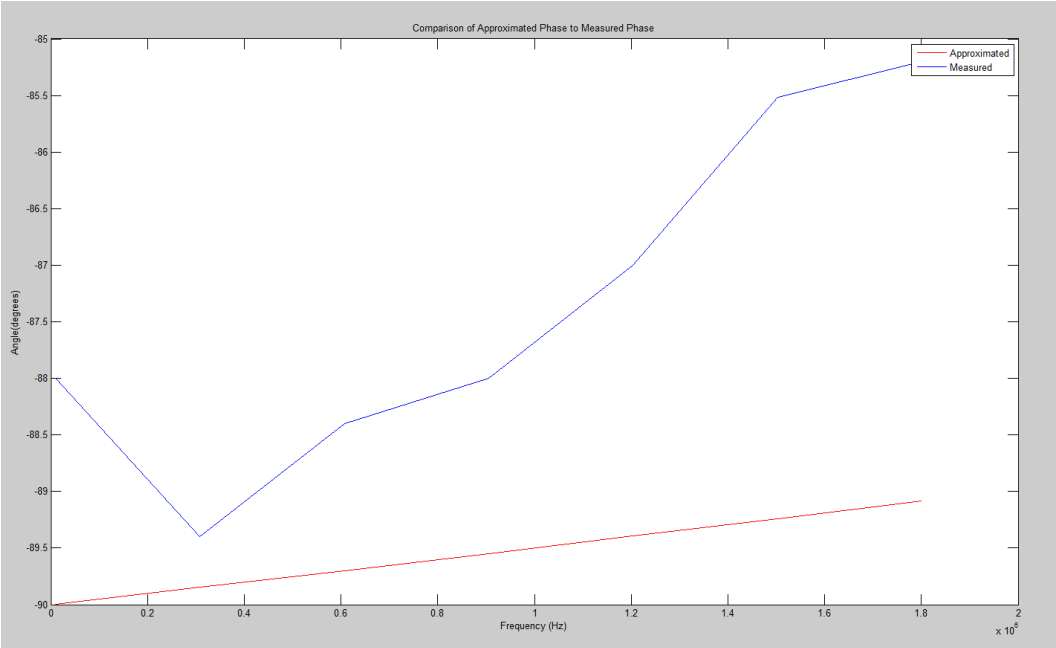


Figure 31 - Plot of Computed Phase (Red) vs. Given Phase (Blue)

Due to the fact that the ultrasound transducer could not be accurately characterized in Figure 30 and Figure 31 with given information, the pulse-shaping module was written generically so future engineers could easily modify the code. The current iteration of the pulse-shaping module simply generates a two-period square wave signal at a frequency of 1.5 MHz with an amplitude of 80V.

Total Hardware Control Interface

Now that all control modules have been discussed, the final implementation that utilizes each individual logic block can be developed. A sequence of events that results in the successful generation of ultrasound pulses using the logic modules is given below:

1. Start the switch bank control module and program the first switch bank. Programming the first switch bank results in connecting the first 16 ultrasound elements to the transmitter circuit.

2. When the switch bank programming is complete, the switch bank control module must send a "programming finished" control signal to the pulser control module

3. After receiving the "programming finished" signal, the pulser control module begins the clock counters on each channel to compute the necessary phases for the signaling scheme.

4. Once each channel reaches the desired time delay, a "pulse begin" control signal is sent to the pulse-shaping module to begin transmitting ultrasound pulses

5. After each channel has finished transmitting pulses, a "pulse finished" control signal is sent to the switch bank control module, which begins the process for the second switch bank (ultrasound elements 17-32).

6. This process is repeated 8 times, once for each switch bank

A graphical representation of the process described above is shown in Figure 32.

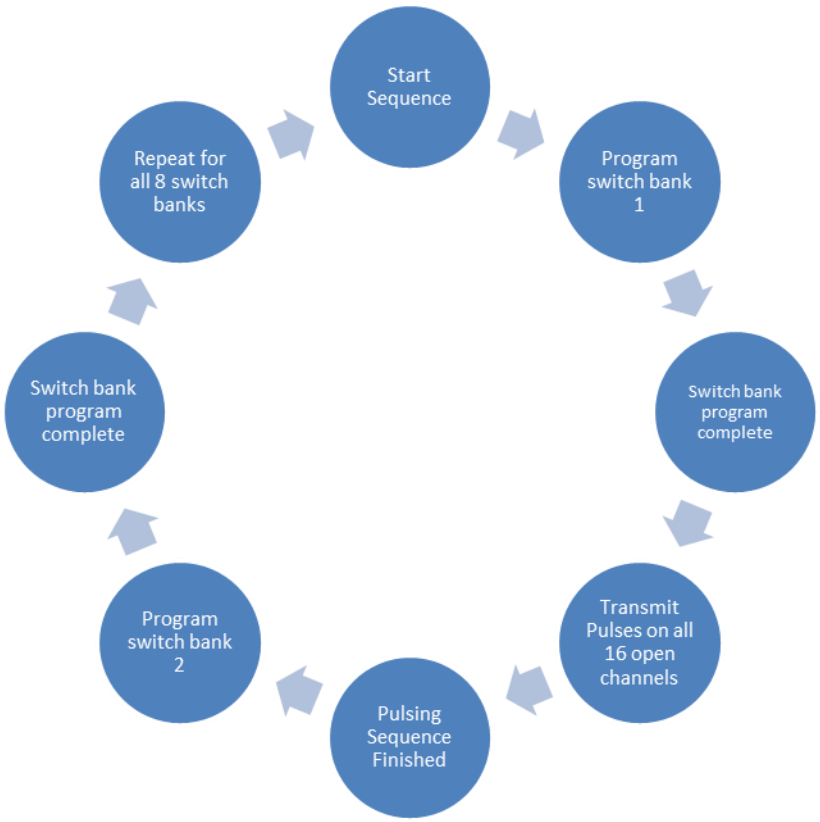


Figure 32 - State Machine Operation

Note: Control signals are not plotted in Figure 32 in order to make the figure more readable and easy to understand from a systems-level.

VHDL code was written in the ISE Design Suite environment to implement the state machine in Figure 32. A simulation result of the state machine is illustrated

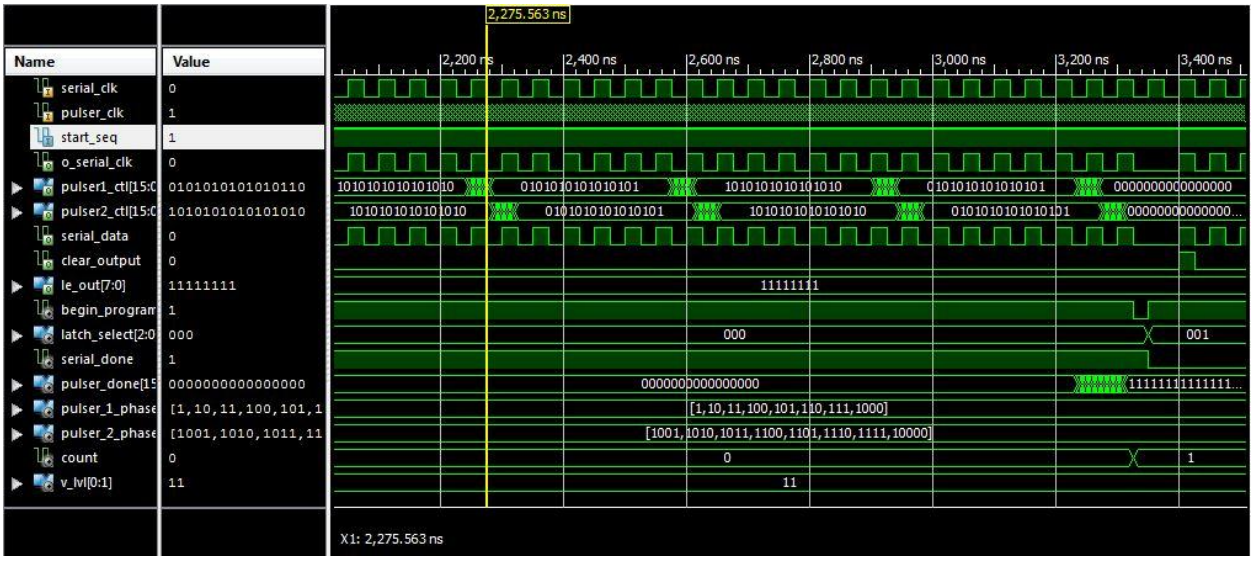


Figure 33 - Transmitter Hardware Control Simulation

The descriptions of several signals of interest in Figure 28 are given below:

- **Serial_clk:** a 20 MHz clock signal generated from the 200 MHz system clock through a clock divider circuit
- **Pulser_clk:** a 200 MHz clock signal obtained from the system clock
- **Start_seq:** a control signal that starts the entire state machine
- **O_serial_clk**: the output 20MHz clock signal to the switch banks
- **Pulser1_ctl:** a vector of 16 bits that control the logic inputs of one pulser IC.
- **Pulser2_ctl:** a vector of 16 bits that control the logic inputs of the second pulser IC
- **Serial_data:** output serial data to the switch banks
- **Clear_output:** the control signal to clear the contents of the latches in the switch banks
- **Le_out**: a vector of 8 bits with each bit mapping to the latch enable input of one switch bank
- **Begin_program**: the control signal for the switch bank module
- **Latch_select:** selects which switch bank to program out of the 8 switch banks
- **Serial_done:** signal that indicates the serial interface has completed programming a switch bank
- **Pulser_done:** a vector of 16 bits that indicates the two 8-output pulser ICs have finished transmitting over the channel
- **Pulser_1_phases:** a vector of information containing the delay for each channel (given in number of 200 MHz clock cycles)
- **Pulser_2_phases**: a vector of information containing the delay for each channel (given in number of 200 MHz clock cycles)
- **Count:** used to run the state machine and keep track of how many switch banks have been programmed and signaled over

The state machine in Figure 33 demonstrates the ability of the FPGA platform to control the transmission of pulses over 128 channels with only a start signal input.

Low-Noise Variable-Gain Amplifier Receiver Hardware

The VGA was acquired by Texas Instruments, the part number is VCA2615. It is a dual-channel system used at the receive end of the ultrasound. Since we need it to accommodate 16 channels, we will use eight VGAs. There are integrated diode bridges that are meant to prevent high-voltage signals from entering the receiver. The amplification stage of the receiver consists of the entire pulse-echo transmitter schematic. The low-noise amplifier/variable-gain amplifier amplifies the heavily attenuated reflected signals, allowing them to be sampled and processed for imaging. This VGA contains a low-noise amplifier (LNP) and a variable-gain amplifier (VGA), which is driven from the LNP. The LNP can be easily programmed to different gains and input impedances. A few of its specifications are listed below:

Parameter	Device Specifications	Required Specifications
VGA Gain	52 dB Gain Control Range	10 – 20 dB Gain
Number of Channels	2	16 channels –8 in our design
LNP & VGA Bandwidth	42 MHz	10 MHz
Supply Voltage	4.75 – 5.25 V	

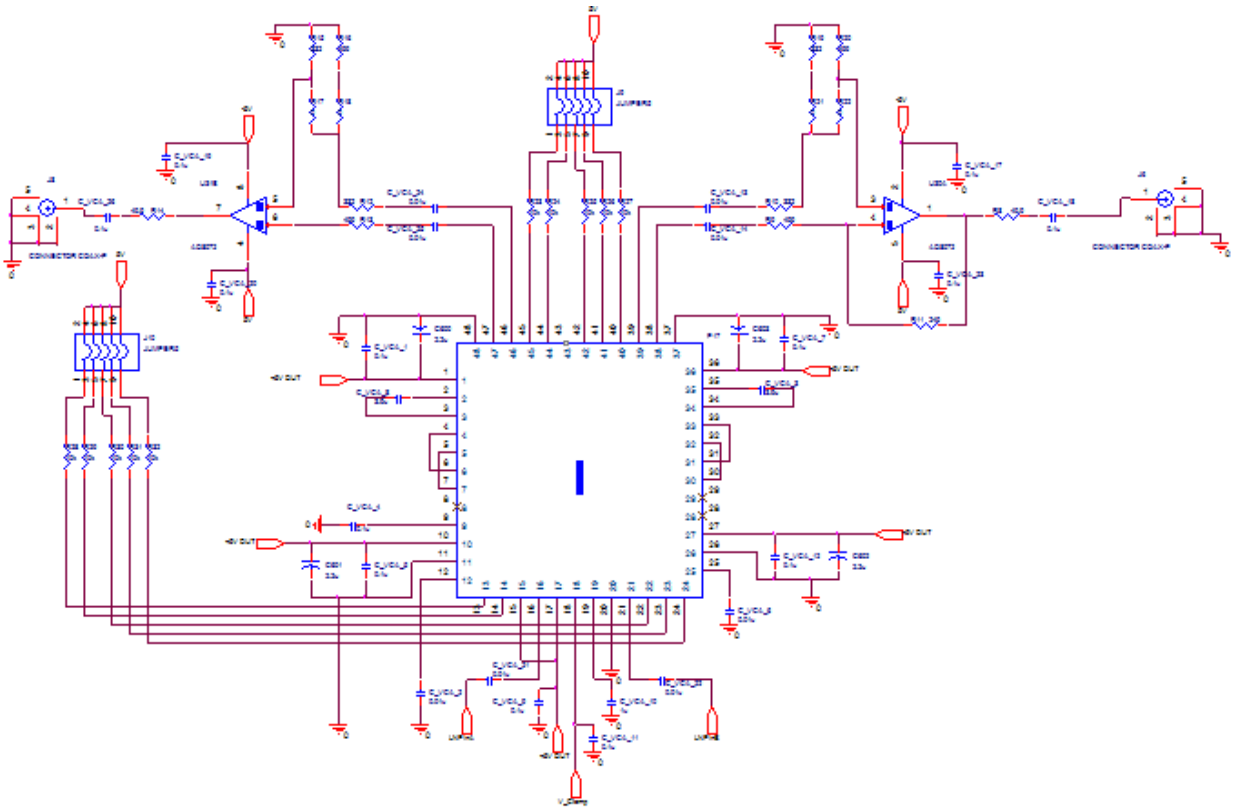


Figure 34 - VGA Test Circuit

Testing and Evaluation

Testing was accomplished through two different methods. The first method was to use PSPICE models for the integrated circuits to run a simulation of the component. However, only a select few of the ICs have PSPICE models available. In this situation a second method was implemented where the integrated circuits are placed on a breadboard to test the functionality and design of the interfaces. The test procedure and results are given below.

1. **Transmitter Test Procedure**
   The two primary components on the transmit side were tested by the use of putting the integrated circuits on a breadboard and checking to see if the components behaved to the specification of their respective datasheets. In both cases, the integrated circuits were setup based off the given information in their datasheets.

HV Pulser Test

1. The circuit was based off the application circuit in the HV Pulser's datasheet and the developed schematic of the pulser shown in Figure 35 .

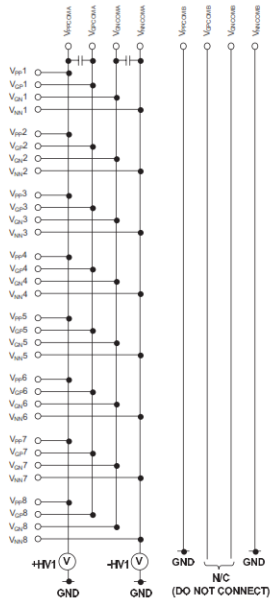


Figure 35 - Pulser Application Circuit

2. Different voltage levels are needed to bias and run the device. Due to this the voltages were applied in a sequence from lowest to highest to prevent damage to the device
   a. 3.3V was applied to V_{LL}
   b. +/- 5V were applied to V_{DD} and V_{SS} respectively
   c. +/- 12V were applied to V_{DD12} and V_{SS12} respectively
   d. +/- 20V were applied to one change of V_{PP} and V_{NN} respectively

3. The logic inputs were tested by applying a pulse from a signal generator
    a. Only one channel was tested at a time
    b. The signal voltage was 5Vpp
    c. The signal frequency was 10k Hz

4. The output signal was measured with an Oscilloscope to see if the waveform was correctly generated.

Results

The circuit shown in Figure 36 was tested multiple times due to issues with the implementation of the application circuit and faulty circuit components i.e. capacitors. These issues short circuited the HV Pulser which meant unsoldering the current pulser and putting a new one on. After going through four different pulsers, the silicon wafer that the pulser was solder to was no longer useable thus ending testing. However, each time a new pulser was tested; more issues were able to be fixed. On the last testing of the pulser, everything ran without short-circuiting the IC but it was not outputting the correct signal. This was attributed to a physical ground that needed to be soldered directly to the thermal pad underneath the pulser which couldn't be reached. A hole was drilled through the wafer which would allow the connection of the physical ground. This final time of unsoldering and soldering the HV Pulser ruined the wafer.

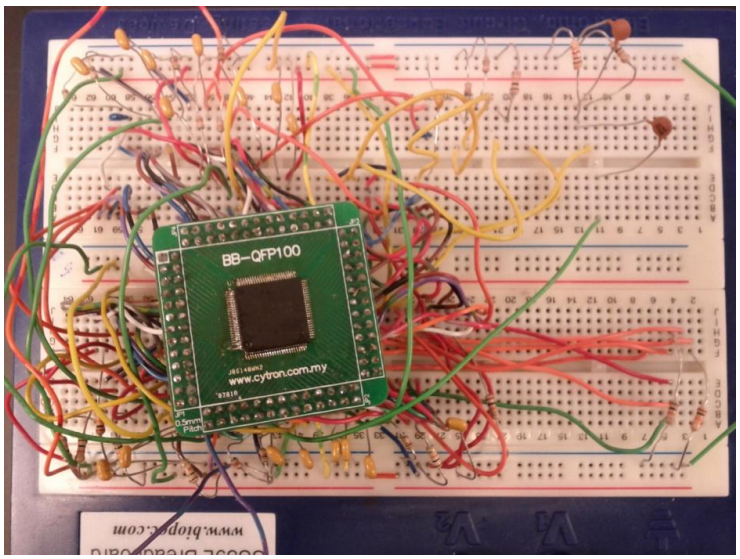


Figure 36 - Breadboarded Pulser Test Circuit

Integrated Switch Bank

Test

1. The breadboard circuit was based off one of the suggested test circuits in the Switch Bank datasheet (shown in Figure 37).

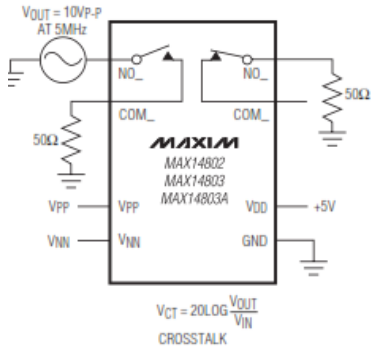


Figure 37 – Suggested Switch Bank Test Circuit

2. Different voltage levels are needed to bias and run the device. Due to this the voltages were applied in a sequence from lowest to highest to prevent damage to the device
    a. 5V was applied to V_{DD}
    b. +/- 20V was applied to V_{PP} and V_{NN} respectively
3. All switches are set to be open by providing a voltage to the Latch Clear Input
4. A wave is provided to the Serial-Clock input
5. A voltage is provided to the Serial-Data input
    a. Individual switches close
6. The channel is tested to see if there is a connection through the switch bank.

Results

The switch bank was tested using the circuit in Figure 38 to see if the switches can be opened and closed in accordance to the datasheet. The switch bank was not tested with the FPGA to keep simplicity with the testing, but a circuit was setup to properly replace the signals that the FPGA would be sending. The switch bank performed how it should of the first try of testing. This is attributed to the relative simple circuit needed to test the IC. If the pulser was still in working condition, the next plan of action would be to chain the two integrated circuits together.

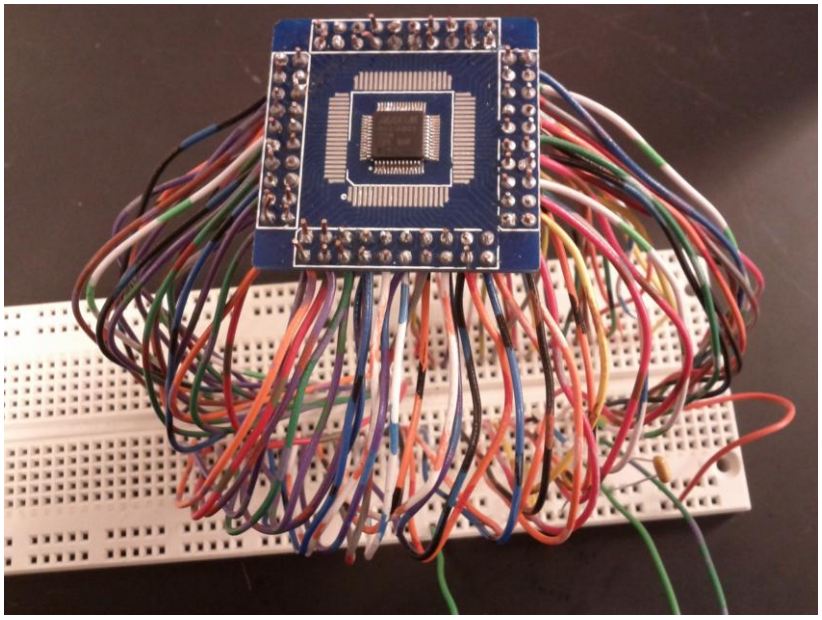


Figure 38 - Switch Bank Test Circuit

2. Power Electronics Testing

To test power regulation a test board must be built. The test board will allow us to test the regulation of the individual components and the external circuitry. There will be tests of individual components and the components combined together. PSPICE simulations were done for the components that had available PSPICE model files.

12VDC Power supply

Requirements

1. 12VDC must be supplied from power source.
2. Power supply connected to Dual Buck converter.
3. Power supply connected to Positive Linear Regulator.

Test

1. Output of power supply is measured at 12VDC.
2. 12VDC is measured at Dual Buck Converter input, PVDD1 & PVDD2.
3. 12VDC is measured at Positive Linear Regulator input Vin.

Dual Buck Converter

Requirements

1. The Dual Buck converter must regulate an output voltage of 5V.
2. The Dual Buck converter must regulate an output voltage of 1.8V.

Test

1. Output of dual buck is measured at 5V.
2. Output of dual buck is measured at 1.8V.

Results

The Dual Buck Converter could not be tested due to the fact some components were not available as a breadboard component

Positive Linear Regulator

Requirements

1. The positive linear regulator must regulate an output voltage of 10V.
2. 10V output must connect to the Inverting Regulator input.

must connect to the HV pulser pin Vdd12.

Test

1. Output of positive linear regulator is measured at 10V.
2. 10V is measured at Inverting regulator input.

Results

The output voltage was connected to a 12 V source and had an output voltage of 10 V. From this test we have concluded that the Linear Regulator worked properly.

Inverting Regulator

Requirements

1. The inverting regulator must regulate an output voltage of -10V.
2. -10V output must connect to the negative linear regulator.

Test

1. Output of inverting regulator is measured at -10V.
2. -10V is measured at negative linear regulator input pin.

Results

The Inverting Regulator could not be tested due to the fact some key components were not available as a breadboard component.

Negative Linear Regulator

Requirements

1. The negative linear regulator must regulate an output voltage of -5V.

Test

1. Output of negative linear regulator is measured at -10V.

Results

The Negative Linear Regulator was connected to a -10V source and had an output voltage of -5 V. The test was successful and verified the Regulator's functionality.

3.3V Linear Regulator

Requirements

1. 3.3V linear regulator must regulate an output voltage of 3.3V.

Test

1. Output of the 3.3V linear regulator is measured at 3.3V.

Results

The 3.3V Linear Regulator was connected to a 5V source and had an output close to 3.3V. Even though the results are not exact, it was concluded that the Regulator was close enough to verify the functionality (shown in Figure 39).

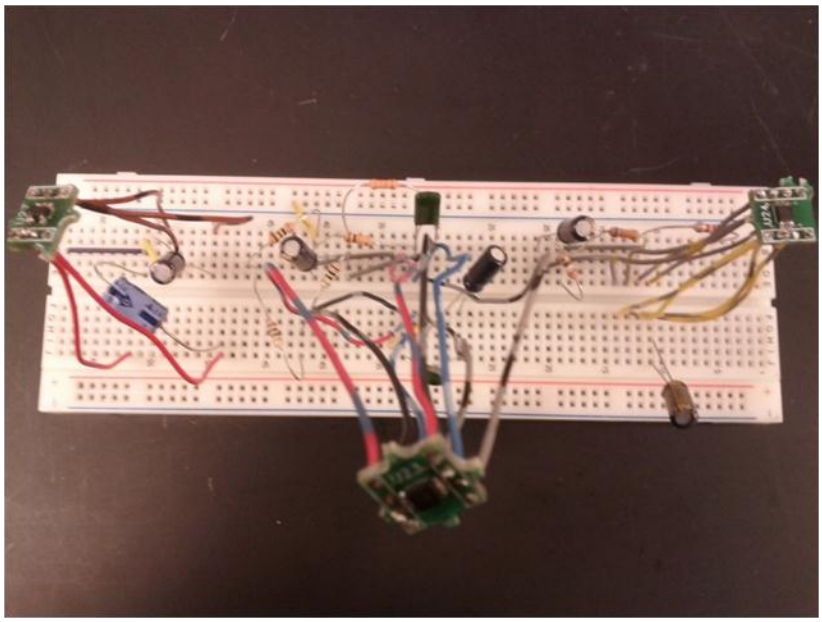


Figure 39 – Power Electronics Test Circuit

Standards

The best source an industry standard for Ultrasounds was in the Code of Federal Regulations under section number 21 CFR 1050.10. It firsts explains all the definitions that are needed to understand the material and then goes into some performance requirements. I have listed the requirements that apply to us below:

1. A means shall be incorporated to indicate the magnitudes of the temporal-average ultrasonic power and the temporal-average effective intensity when emission is of continuous-wave waveform.
2. A means shall be incorporated to enable the duration of emission of ultrasonic radiation for treatment to be preset and such means shall terminate emission at the end of the preset time. Means shall also be incorporated to enable termination of emission at any time. Means shall be incorporated to indicate the magnitude of the duration of emission.
3. A means shall be incorporated for indicating the magnitudes of pulse duration and pulse repetition rate of the emitted ultrasonic radiation, if there are operation controls for varying these quantities.
4. A means shall be incorporated to provide a clear, distinct, and readily understood visual indicator when and only when electrical energy of appropriate ultrasonic frequency is being applied to the ultrasonic transducer.

The next sub index of this section describes where and how labels should be fixed to the ultrasound. All of

the controls need to have a label explaining what each control does and how to use it. The waveform generator must also have a label fixed on it. The specifications for labels are listed below:

> Labels required by this paragraph shall be permanently affixed to or inscribed on the ultrasonic therapy product; they shall be legible and clearly visible. If the size, configuration, or design of the ultrasonic therapy product would preclude compliance with the requirements of this paragraph, the Director, Center for Devices and Radiological Health, may approve alternate means of providing such labels.

The last part of this section explains what information must be explained by the manufacturer of the ultrasound. It is listed below:

1. Adequate instructions concerning assembly, operation, safe use, any safety procedures and precautions that may be necessary regarding the use of ultrasonic radiation, and a schedule of maintenance necessary to keep the equipment in compliance with this section.
2. Adequate description of the spatial distribution of the ultrasonic radiation field and the orientation of the field with respect to the applicator. This will include a textual discussion with diagrams, plots, or photographs representative of the beam pattern.
3. Adequate description, as appropriate to the product, of the uncertainties in magnitude expressed in terms of percentage error, of the ultrasonic frequency effective radiating area, and, where applicable, the ratio of the temporal-maximum effective intensity to the temporal-average effective intensity, pulse duration, pulse repetition rate, focal area, and focal length.
4. A listing of controls, adjustments, and procedures for operation and maintenance, including the warning "Caution—use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous exposure to ultrasonic energy."

These standards produced by the federal government ensure that the ultrasound is used properly.

Future Work

The intention of the client is to expand upon the work done by our group and implement control over 512 ultrasound transducer elements. However, the many same concepts including pulse-width-modulation for amplitude control and FPGA transmitter control employed by our group will be used in the future iterations of the system. It will be important to future senior design teams to immediately begin prototyping smaller parts of the ultrasound system presented in this report to understand the system and the necessary interfaces between each component. Restrictions in time and budget prevented our group from thoroughly prototyping individual blocks of the design to ensure correct functionality, and we believe significant insight could be developed doing so.

Our team also invested a significant amount of time researching pulse-echo ultrasound theory and finding components that would allow us to meet the design requirements during the first semester of the project. Several different alternatives for implementing the amplitude and phase control of our transmitter were thoroughly investigated, and we believe that we picked the simplest and most flexible approach to solving these challenging problems. Future senior design groups will have the ability to primarily focus on low-level design and challenges with implementing the designs due to the research presented in this report. The

research done during this project also includes a cost analysis of fabricating the large ultrasound circuits, and significant work can be done on modularizing the design into smaller boards to reduce fabrication costs.

In order to modularize the design, the ultrasound transmitter circuit can be split into functional blocks that and fabricated on their own PCBs. However - it is challenging to fit even small portions of the current circuit onto a 60 square inch board, which is the maximum PCB size that receives the academic discount. Many of the integrated circuits utilized in the design have pin counts ranging from 48-100, and fitting the traces between these circuits on two layers was problematic for our team. Additionally, high-pin-density connectors that can handle 80V signals and currents ranging from 0-3A on each pin will be necessary to carry the numerous signals between modular boards. Overall, our group suggests pursuing the route of fabricating small circuits and understanding their operation before pursuing any expansion activities.

Operation Manual

The purpose of this section of the report is to document how to connect and operate the different components of the system. Due to significant challenges with implementing the pulse-echo ultrasound system by then end of the semester, many of the components were not fabricated in time to be tested thoroughly. However, our team has a through understanding of the system and how the different subsystems should operate. The operation manual is based upon this understanding.

Preparing the System

1. In order to supply power to all of the components in the ultrasound transmitter, the power regulation board should be activated first.

2. In order to prepare the power board for operation, locate the power output connectors located on the board (highlighted in Figure 40)

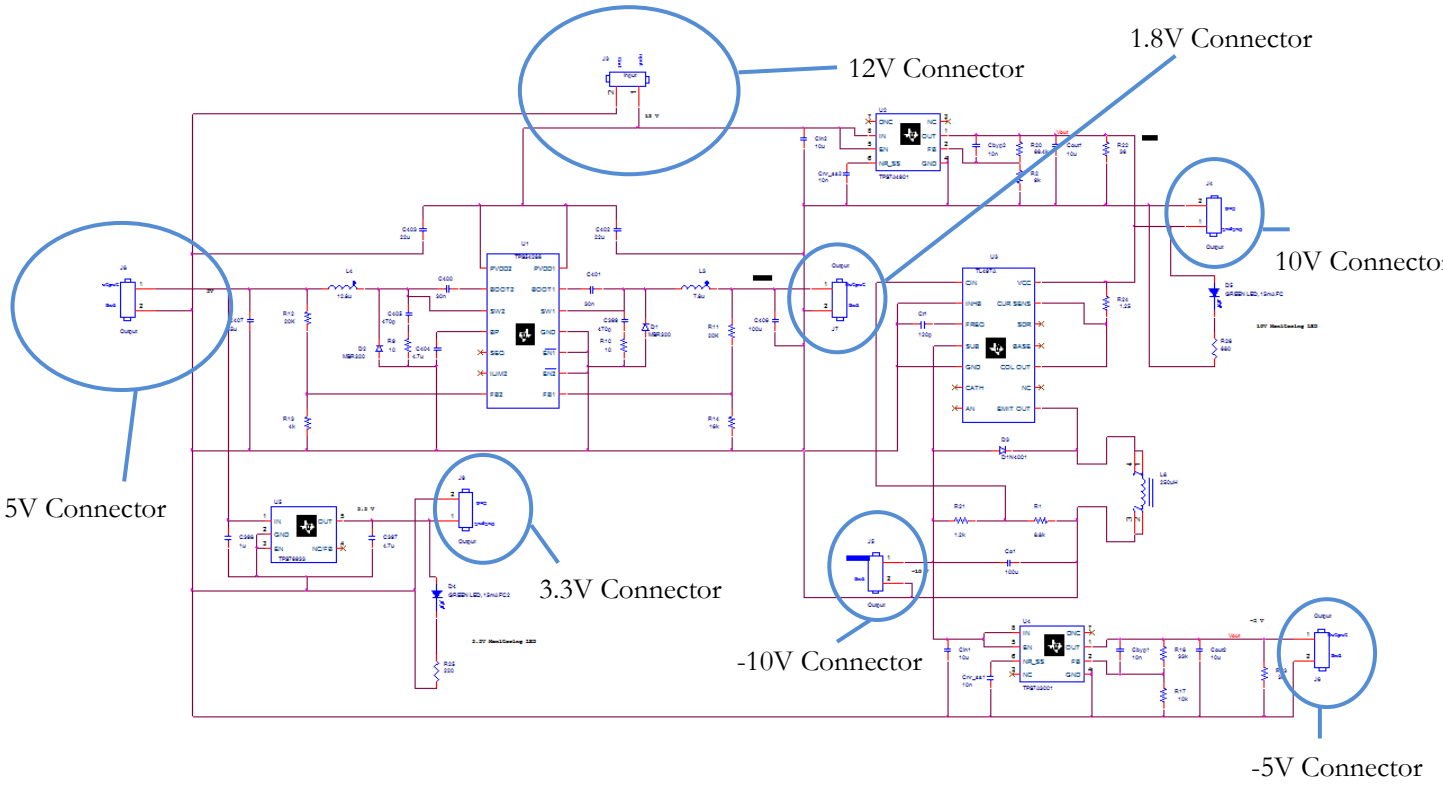


Figure 40 - Identifying Power Connectors on the Power Electronics Board

3. First, connect the 12V header connector to the 12V system power supply. If the board LEDs illuminate after this connection, the board is correctly regulating the 12V supply down to the various voltages needed within the system.

4. Unplug the 12V connector and connect each supply output to the mating end on the ultrasound transmitter PCB. Each connector on the ultrasound PCB will be labeled with the expected voltage source.

5. It is now time to set up the FPGA interface to the ultrasound transmit PCB. Identify the FMC low-pin count connector on the ML605 evaluation board (highlighted in Figure 41). Plug the FPGA interface PCB into this connector and secure the screws on the board.

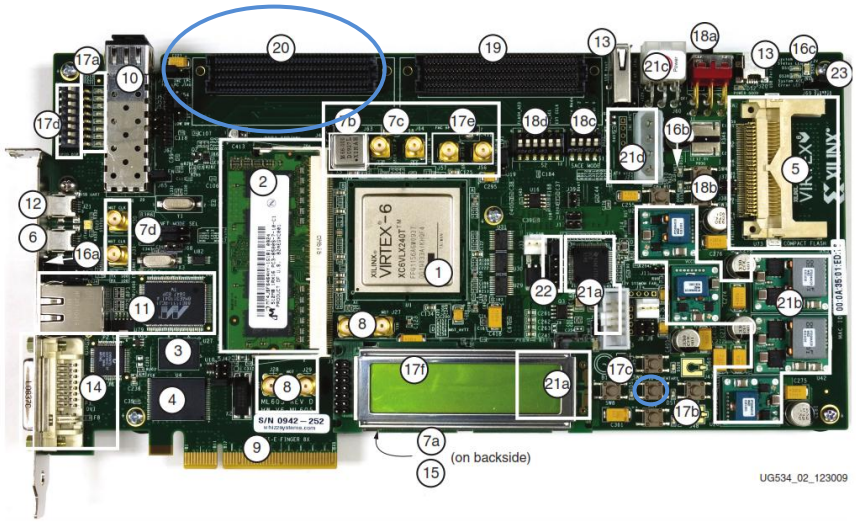


Figure 41 - Low-Pin Count Connector Location on ML605 Board

6. Next, the FPGA will need to be turned on and programmed with the correct channel phase configuration. A PC user interface has not been fully developed to allow for users to modify these values, so the information must be entered manually in the VHDL code.

7. In order to enter the phase information, open Xilinx ISE and navigate to the file named "Transmitter_Control.vhd". The channel phase information is contained in two integer vectors named "pulser_1_phases" and "pulser_2_phases". After the correct phase information has been entered, compile the VHDL project in to a bitstream and upload the design onto the Virtex 6 FPGA. After uploading the design, the two LEDs on the FPGA interface board should be illuminated.

8. A load needs to be provided to the outputs of the transmitter to prevent high-voltage pulses from dissipating energy in the switch bank ICs and other components through wave reflections. Ensure that the ultrasound probe connector (wired to the ultrasound transmitter board) is connected to an ultrasound transducer that is placed in a beaker of water.

9. Connect the 12V supply connector to the power regulation board to provide supply voltages to the ICs on the ultrasound transmitter board. Next, connect the high-voltage supply to the ultrasound transmitter board while following safety procedures regarding the handling of high-voltage circuits.

10. With all power supplies and FPGA control interface connected to the ultrasound transmitter board, the system is now ready to transmit pulses to the output interface. Press the middle push-button on the ML605 board (highlighted in Figure 41) to begin the pulsing sequence.

Appendix - Receiver System Overview

Only the transmitter circuit and functionality has been described up to this point in the document due to the fact that the transmitter design was the only deliverable solution of our project. During the first semester of work, we evaluated the receiver design and selected components that would meet the design requirements. An overview of this evaluation is given below.

The objective of pulse-echo ultrasound is to acquire reflected pulse signals in order to obtain a good view of the brain. An outline of the receiver design in shown below in Figure 42.

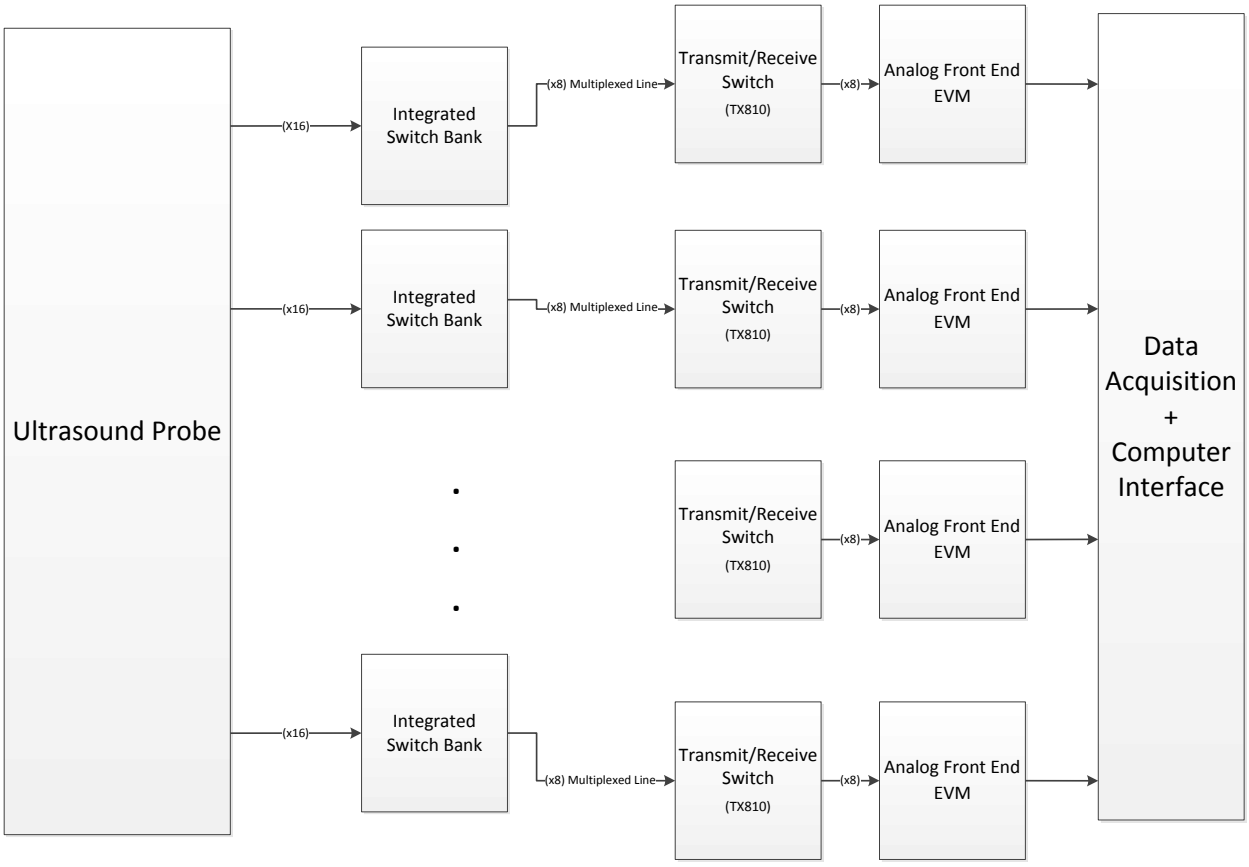


Figure 42 - Ultrasound Receiver Block Diagram

Figure 42 details multiple interfaces between components, and the objective of the next section is to explain the functionality of each component and its interface to other devices.

Integrated Switch Bank

This component was discussed thoroughly in the previous section that described the transmitter operation. Please refer to this section for details.

Transmit/Receive Switch

Ultrasound pulses must be both sent and received through the same channels of the transducer in order for the system to function. Therefore, a method of protecting the receiver from the high-voltage signals being sent by the transmitter must be devised. Fortunately, Texas Instruments has developed an integrated circuit (the TX810) that incorporates diode bridges for eight channels into a single package. The equivalent circuit for this device is shown in Figure 43.

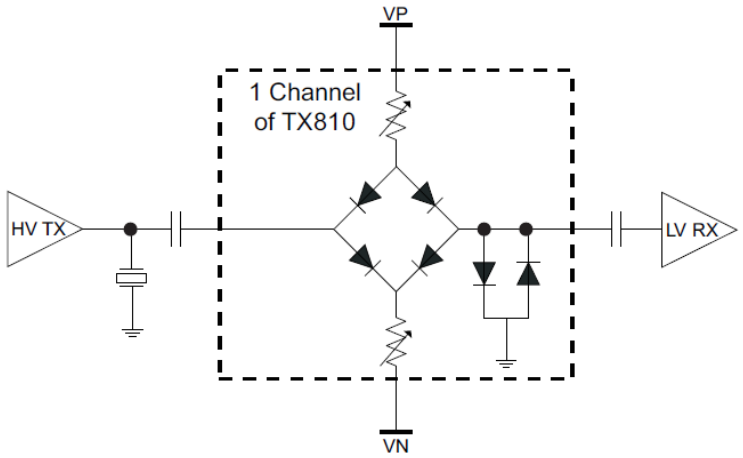


Figure 43 - Equivalent Circuit of the TX810 Transmit/Receive Switch

By observing the circuit in Figure 43, it can be seen that signals with a magnitude greater than VP and VN will not be passed to the "LV RX" pins. Therefore, this device will only allow small-amplitude signals to pass to the receiver.

Analog Front End

The Analog Front End is an integrated circuit, manufactured by Texas Instruments, that incorporates all of the functions needed to recover an ultrasonic pulse into a single package. An equivalent circuit of the device is shown below.

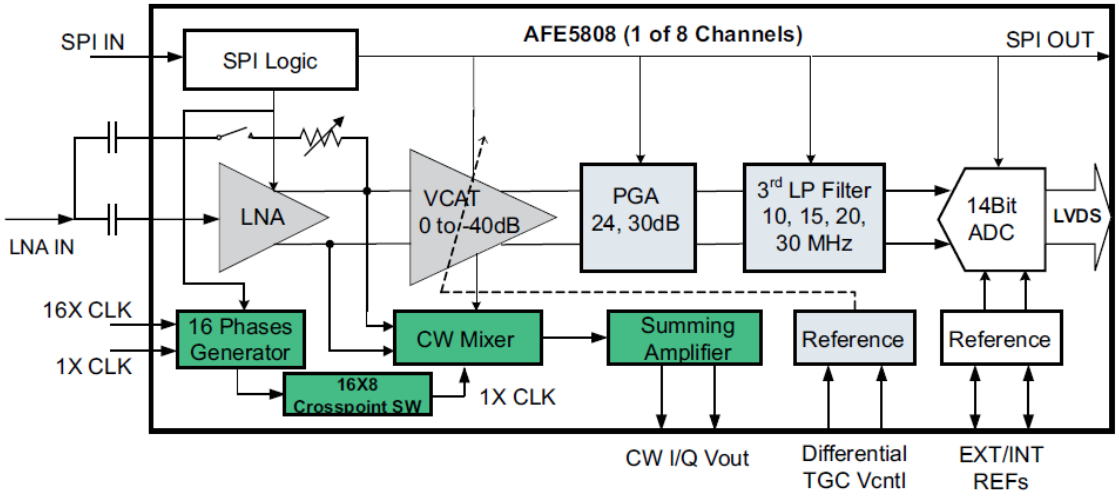


Figure 44 - Equivalent Circuit of One Channel of The AFE5808

While the device itself incorporates a significant amount of functionality into one package, our team has elected to purchase a set of evaluation boards that contain the device. These evaluation boards have all of the interfaces to the AFE5808 broken out so it can be easily incorporated into the existing ultrasound system design.
With using the AFE5808EVM as the analog front end on its own, the team will able to also use the test features of the board. The main features of this are

- Continuous wave test
- 8 channel low-voltage differential signal (LVDS) outputs from the ADC

Along with using the test features built into the AFE5808, we will be using the TSW1250EVM to further test and analyze the AFE5808. The AFE5808 and TSW1250EVM are pictured below in Figure 45.

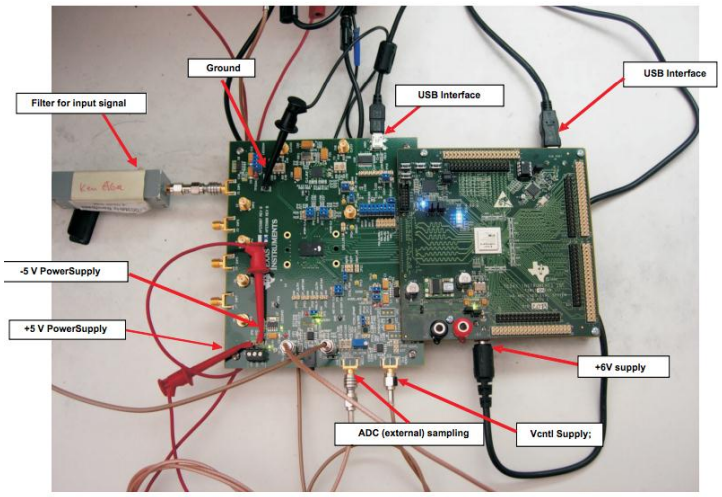


Figure 45 - Image of a Test Set-up for the Analog Front End Evaluation Module

The TSW1250EVM connects directly into the AFE5808 and can analyze the AFE5808's LVDS data stream. The TSW1250EVM interfaces to a computer, much like the AFE5808, through USB and has GUI software that is provided with the board. The main features of the board are

- High-speed ADC with LVDS output
- 64k capture depth with USB transfer

The evaluation boards and GUI provide an effective way to demonstrate that the AFE5808 is performing at expected data sheet specifications.

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