Photolithography Mask Design

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Background: EE432/532

• EE 432/532 is a microelectronics fabrication class
  – Popular class
• Make a silicon wafer with devices including MOSFET and BJT
  – in an educational purpose class
• A hands on class with lab at Applied Science Complex
  – Diffusion
  – Oxidation
  – Photolithography
    • mask
  – Evaporation
  – And more
Photolithography

Exposure of UV light to photoresist with mask

Photoresist is washed away using acetone

Removal of oxide in exposed regions
Bare Wafer

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Pattern PWELL

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Pattern PMOS Source/Drain
Pattern NMOS Source/Drain
Pattern Contacts

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Apply Metal to Entire Wafer
Pattern Metal

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Problem Statement

• No transistors functioned from the summer 2012 EE 432/532 class

• Problem with old photolithography masks
  – Devices are too small and too close together
  – Mask alignment marks are small and hard to find
  – Wafer space not utilized
Scope

• Design a set of photolithography masks (six) that can be used in the EE 432 lab

• The EE 432 process outside of the masks stays the same

• Use L-Edit (CAD tool) to design the masks
Deliverables

• A set of six photolithography masks

• Mask documentation for student use

• A set of fabricated wafers to test
Initial Design

• Rough sketch of transistor
L-Edit Design

- Current Actual transistor design
- Each dot represents 2.5um
Fabricated Transistor
Die Design

- One die (a set of transistor, e.g. an Intel CPU core)
- 39 devices per die
- 9 different devices per die
- Devices include MOSFET, BJT, VDP, capacitors, TLM (resistor), and logic gates
Alignment Marks

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Alignment Marks Walkthrough

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Alignment Marks Walkthrough
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Alignment Marks Walkthrough
Alignment Marks Walkthrough
Fabricated Alignment Marks
Alignment Machine

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Mask Design

- The entire mask has 37 die
- A ring around all the dies
  - Helps align the mask with the alignment machine.
Challenges

• Problem: The masks cannot be tested before fabrication

• Solution: Spending extra time in the design phase working on analysis. We got each design approved by our advisor before getting any masks fabricated
Challenges

• Problem: Developing a set of design rules for the devices

• Solution: We spent time looking at the old design, and looked for areas where they may not have left enough spacing. We met with our advisor to approve all design rules.
Challenges

• Problem: Working with new software (L-Edit)
• Solution: Used our experience with similar software (Cadence). We spent some time going through the L-Edit documentation to better use the software features.
Testing

• A set of wafers have been fabricated using the new mask set
  – Alignment successful
  – Functional transistors
  – More space utilized
Testing

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Testing
Testing

NMOS IV Curve

IDS (Amps)

VDS (Volts)

VGS = 0V
VGS = 1V
VGS = 2V
VGS = 3V
VGS = 4V
VGS = 5V

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What Worked

• All groups had working NMOS transistors
• Most NMOS transistors worked except for the smallest (5 micron length)
• Over half the groups had working PMOS transistors
Transistor Results

• NMOS
  – Threshold voltage ranged from 2.4 to 2.9 volts
• PMOS
  – Threshold voltage ranged from -1.4 to -1.7 volts
• TLM Pattern
  – Showed contacts where ohmic with $V=IR$ relationship
1-29-2013
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Questions?